Design Guide: TIDA-010272

1500V High-Voltage Rack Monitor Unit Reference Design for Energy Storage Systems

Description

This reference design is a high-voltage, current and insulation impedance accuracy lithium-ion (Li-ion), LiFePO4 battery rack. The design monitors four high-voltage bus inputs, one shunt current and temperature, and one insulation impedance of the battery. The design protects the battery rack to maintain safe operation. The design provides an onboard serial peripheral interface (SPI) and off-board daisy-chain communication interface, allowing for a cost-effective stackable connection and reinforced isolation. These features make this reference design applicable for high-capacity battery rack applications.

Resources

TIDA-010272	Design Folder
BQ79731-Q1, TPSI2140-Q1	Product Folder
SN6507, ISO7841	Product Folder
SN74LVC1G07-Q1, TPS7B69-Q1	Product Folder
TSD05C, ESDS552	Product Folder

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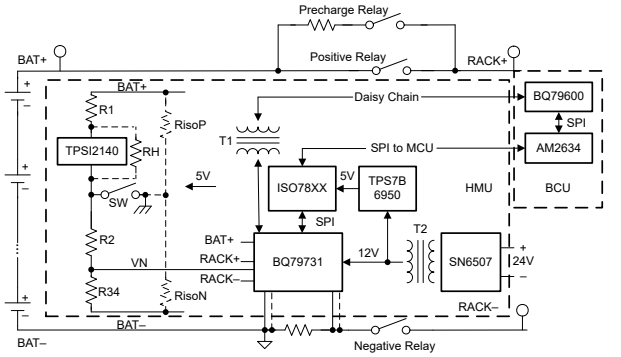
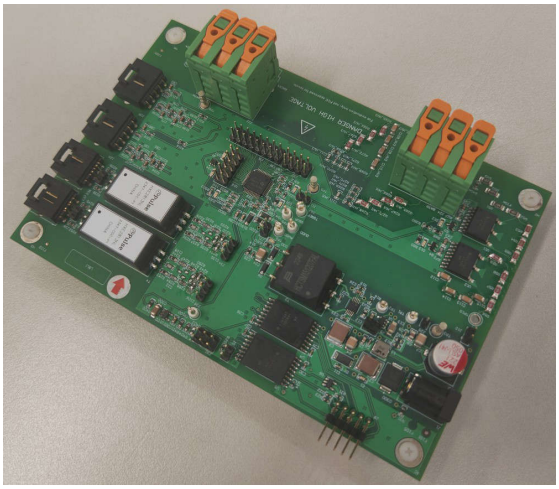
Features

- ±0.5% bus voltage accuracy at 25°C
- ±10mA at 25°C, < 10A; ±0.1% error at 25°C, > 10A of shunt current
- Supports shunt temperature calibrations
- ±20% error at 25°C, 50kΩ to 10MΩ; ±10kΩ, < 50kΩ of insulation impedance
- Robust daisy-chain communication with data reclocking and ring architecture
- Redundant diagnostics for rack current, voltage measurement, and protections

Applications

- ESS – Battery management system (BMS)





1 System Description

A Battery Energy Storage System (BESS) is a technology that stores electrical energy in the form of chemical energy within batteries. This stored energy can be later converted back into electricity and released when needed. BESS plays a crucial role in enhancing the reliability, stability, and efficiency of electrical power systems.

A BESS often consists of multiple battery racks arranged in a modular and scalable manner to meet the energy storage needs of a particular application. Each rack within a BESS typically includes a set of batteries, a battery management System (BMS), and associated hardware to facilitate energy storage, monitoring, and control. Battery racks are the physical structures that house the individual batteries. Battery racks provide a secure and organized framework for mounting the batteries, maintaining stability, and safety. The number of battery racks in a BESS depends on the required capacity and the specific design of the energy storage system.

The high-voltage monitor unit (HMU) part of a BMS is a critical component that focuses on managing and maintaining the safety of the high-voltage aspects of a battery pack. The following items are key elements typically found in the high-voltage part of a high-voltage BMS:

1. Voltage measurement: BMS includes specialized circuits to measure the voltage of individual battery cells or modules within the high-voltage battery pack. Accurate voltage monitoring is crucial for maintaining the health and safety of the battery system.
2. Current measurement: Current sensors are integrated into the high-voltage circuit to measure the charging and discharging currents of the battery pack. This information is essential for state-of-charge estimation and preventing overcurrent conditions.
3. Insulation impedance monitoring devices: Instruments that monitor the isolation integrity of the high-voltage components to detect and prevent isolation failures.
4. Communication interface: Interfaces such as Controller Area Network (CAN), or other communication protocols, allow the high-voltage BMS to exchange information with other parts of the vehicle or energy storage system.
5. Isolation devices: Devices providing electrical isolation between the high-voltage battery and the rest of the BMS control electronics. This isolation is crucial for safety and preventing electrical interference.
6. Emergency shutdown mechanisms: Emergency shutdown features can be implemented to rapidly disconnect the high-voltage battery pack in critical situations, maintaining the safety of the system and personnel.

These components collectively form the high-voltage part of a BMS, enabling precise monitoring, control, and protection of the high-voltage battery pack in applications like electric vehicles or large-scale energy storage systems.

This design focuses on high-voltage monitoring of large capacity battery rack applications, which can be applied in residential, commercial, industrial, grid BESS, and more. The design uses one BQ79731-Q1(battery junction box voltage monitor, current sensor, and isolation impedance sensor) device to measure four bus voltages and one shunt current. The design uses the TPSI2140-Q1 device and reed relay in a high-voltage, side-grounded, unbalanced bridge to calculate a precise insulation impedance of BESS up to 1500V. The design uses the SN6507 device and the transformer to convert 24V in the low-voltage side to 12V in the high-voltage side.

The design achieves the 1500V reinforced insulation requirement of UL1973 or IEC60664-1-2020. Wide-body isolation products including the digital isolator ISO7841DWWR, a transformer, and a ladder of resistors are used in consideration of the reinforced insulation requirement.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the high-voltage BMS block diagram. BMS is divided into three individual reference designs: TIDA-010271 for the battery monitor unit (BMU) in pack, TIDA-010253 for the battery control unit (BCU), and TIDA-010272 for the high-voltage monitor unit (HMU).

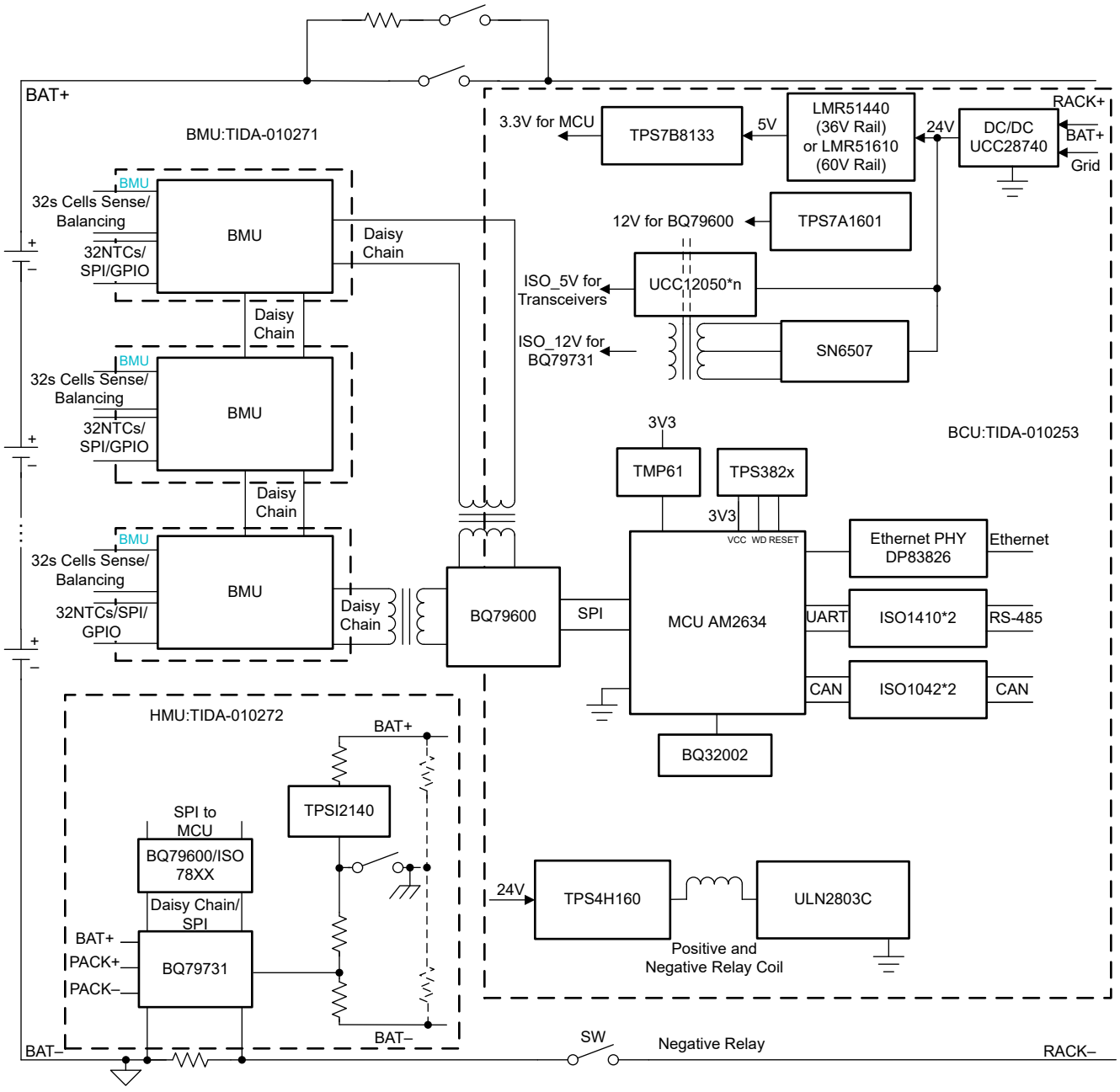


Figure 2-1. BMS Block Diagram

Figure 2-2 shows the TIDA-010272 block diagram. BQ79731 uses four channels of general purpose input/output (GPIO) and VF analog-to-digital converter (ADC) inputs to measure the test point of BAT+, RACK+, RACK–, and VN. VN is voltage between PE and BAT–. The resistor ladders are designed with 1500V bus voltage and the input range of ADC reference.

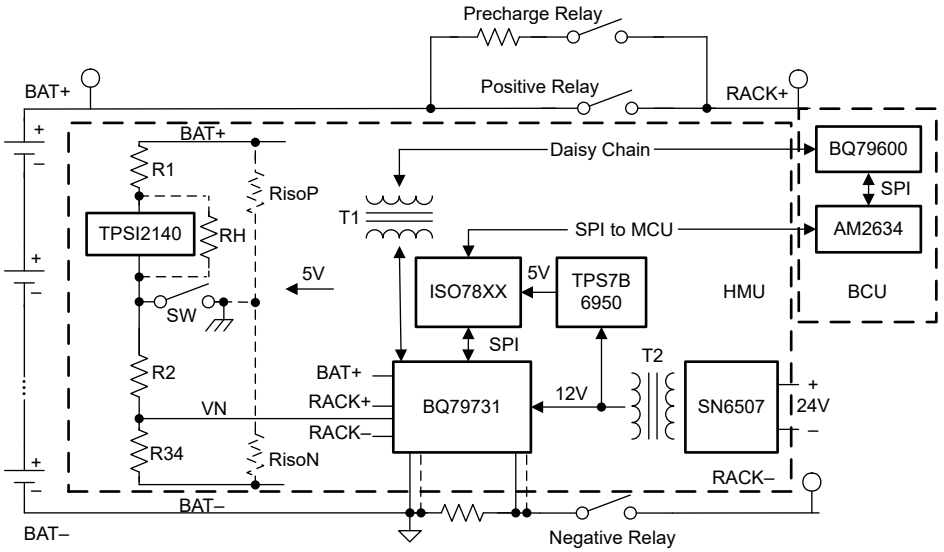


Figure 2-2. TIDA-010272 Block Diagram

The BQ79731 device provides two separate channels of current sense ADC (CSADC) to measure the shunt current. The shunt is not mounted on the board, requiring a real shunt or shunt simulator to give out the differential cross voltage to CSADC input. The BQ79731 also provides two thermistor inputs to enable the calibration of temperature shift either for shunt or CSADC.

The BQ79731, TPSI2140, and switch (SW) together, and form an asymmetric insulation impedance detection circuit. The high-side TPSI2140 is used to change the resistance between BAT+ and PE by adding or not adding the RH resistor, which can create two equations between RisoP, RisoN, VN, and VBAT. VBAT is the rack voltage. VN and VBAT can be measured in a switching duty cycle of TPSI2140. This can enable the calculation of RisoP and RisoN.

2.2 Design Considerations

2.2.1 Accuracy of Bus Voltage Measuring

Bus voltage measuring is a common function in high-voltage BMS. In Figure 2-1, there are three bus voltages including BAT+, RACK+, and RACK– to be measured. Bus voltage is used in the process of state-of-charge (SoC) estimation, precharge, wielding detection, and overvoltage protection. The design target accuracy is 0.5% while 1%, is required in GBT34131-2023.

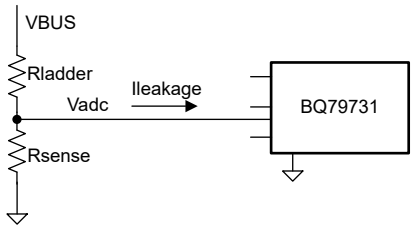


Figure 2-3. High-Voltage Measuring Circuit

Figure 2-3 shows the high-voltage measuring circuit. The measuring circuit contains Rladder, Rsense, and ADC (BQ79731). $I_{leakage}$ is the differential leakage current to ADC input of BQ79731. The accuracy of bus voltage measuring is affected by the error rate of R_{ladder} (R_{ladder}%), R_{sense} (R_{sense}%), $I_{leakage}$, and error of ADC (V_{eadc}).

The actual bus voltage measured with the BQ79731 is $Vbus_{mea}$, and $Vbus_{mea}$ = Vbus + V_{error}. V_{error} can be estimated as shown in Equation 1.

$$\text{Verror} \approx \text{Vbus} \times \left(\frac{\text{Rsense\%} - \text{Rladder\%}}{1 + \text{Rladder\%}}\right) + \frac{\text{Veadc} \times (\text{Rladder} + \text{Rsense})}{\text{Rsense}} + \text{Ileakage} \times (\text{Rladder} + \text{Rsense}) \times (1 + \text{Rsense\%}) \quad (1)$$

Constant error is caused by V_{eadc} and $I_{leakage}$ which does not dominate the error if the V_{eadc} and $I_{leakage}$ is small enough. V_{eadc} of BQ79731 VF and GPIO is ±3.16mV maximum from –40°C to 125°C. $I_{leakage}$ of BQ79731 VF and GPIO is 20nA maximum from –40°C to 105°C. Considering 1500V BESS, voltage gain ≤ 400, and R_{ladder} + R_{sense} ≤ 10MΩ. Then the constant error is less than 1.464V in 1500V ESS. This constant error is too small to be ignored or easily calibrated. The proportional error is related with Rsense% and Rladder%. Assuming the Rsense% and Rladder% are in range of ±1%. The worst case, the proportional error is in a range of ±2%. The proportional error can also be calibrated. If no calibration is used, the ±0.2% accuracy resistors must be used to achieve the ±0.4% accuracy of bus voltage measuring.

In this design, Rladder% and Rsense% are ±1%, Rladder is 6MΩ and Rsense is 16.63kΩ. This considers a basic isolation and creepage requirement of 7.6mm and the usage of four 1206 package Bourns® high-voltage resistors.

2.2.2 Shunt Current Measuring

The shunt current accuracy is a key parameter to calculate the SoC of the battery. The target shunt accuracy of this design is 0.1% when the current is no less than 10A, and maximum 10mA error when the current is less than 10A at room temperature. The shunt resistance is 150µΩ and current range is ±500A. A maximum of 10mA across the 150µΩ error when current is less than 10A requires the maximum error of CSADC to be less than 1.5µV when shunt voltage is less than 1500µV. The gain error of CSADC after calibration must be smaller than 0.1% or less.

The shunt resistance has temperature drift. The shunt resistance needs three test points to calculate the resistance-temperature curve and costs several minutes to get the stable shunt temperature. Some shunt manufactures can provide a resistance temperature curve for each shunt like the PCBS8518A050Q2AC00 device from C&B Electronics. Resistance temperature curve can be used to estimate $R_{shunt}(T)$ (shunt resistance in temperature T).

The shunt calibration process in end-of-rack production line at room temperature:

1. Current = 0A, read the CSADC data V_{CSADC0}
2. Current = 10A or larger
   - Read the CSADC data V_{CSADC0}
   - Read the current $I_{CSADC10}$, calculate the shunt voltage $I_{CSADC10}$ multiplied by $R_{shunt}(T)$
3. Calculate the offset. Offset = V_{CSADC0}.
4. Calculate the gain. Gain= ($I_{CSADC10}$ × $R_{shunt}(T)$ – Offset) / ($I_{CSADC10}$ × $R_{shunt}(T)$).
5. Write offset and gain to EEPROM and flash

2.2.3 Insulation Impedance Monitor

The design uses the asymmetric bridge topology to achieve an accuracy of ±20% when insulation impedance (RisoP and RisoN) is no less than 50kΩ, and 10kΩ maximum error when insulation impedance is less than 50kΩ.

SW is the switch to connect PE and the isolation impedance monitor circuit. SW is switched on once the isolation impedance monitor function starts. To get a high accuracy isolation impedance, use the following several steps:

1. Turn SW and TPSI2140 off. BQ79731 measures the BUS voltage VDC (VBAT+ – VBAT–).
2. Turn SW and TPSI2140 off. Resistor RH is in series with resistor R1. BQ79731 measures the voltage VNoff from PE to BAT–.
3. Turn SW and TPSI2140 on. Resistor RH is short-circuited. BQ79731 measures the voltage VNon from PE to BAT–.
4. Calculate the RisoP and RisoN.
5. Return to step 1 to continue a new monitoring cycle.

Figure 2-4 shows insulation impedance monitor circuit. The working voltage across the TPSI2140 contact is designed to be kept under 1000V with the paralleled the resistor RH and series R1. RH is 1.5MΩ and R1 is 3MΩ. RH and R1 are 0.1% accuracy resistors. R2 is 4.5MΩ with 0.1% accuracy. In the worst-case scenario that RisoN is short-circuited and TPSI2140 is switched off, R1, RH and TPSI2140 together endure all bus voltage. In this case, the voltage across the TPSI2140 is 1000V.

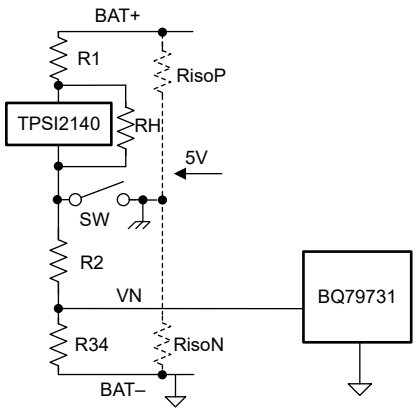


Figure 2-4. Insulation Impedance Monitor Circuit

In step 1 through 3, VDC, VNoff, and VNon can be measured with BQ79731 and can be calculated using Equation 2 and Equation 3.

$$\mathrm{RisoP} = \frac{\mathrm{VDC} \times (\mathrm{VNon} - \mathrm{VNoff})}{\frac{(\mathrm{VDC} - \mathrm{VNon}) \times \mathrm{VNoff}}{\mathrm{R1}} - \frac{(\mathrm{VDC} - \mathrm{VNoff}) \times \mathrm{VNon}}{\mathrm{R1} + \mathrm{RH}}} \tag{2}$$

$$\mathrm{RisoN} = \frac{\mathrm{VNon}}{(\mathrm{VDC} - \mathrm{VNon})\left(\frac{1}{\mathrm{R1}} + \frac{1}{\mathrm{RisoP}}\right) - \mathrm{VNon} \times \frac{1}{\mathrm{R34} + \mathrm{R2}}} \tag{3}$$

The accuracy of calculating can be as high as 10% when RisoP and RisoN are in range from 50kΩ to 10MΩ at room temperature.

In consideration of ADC error and resistor error, the worst case of insulation impedance estimation is 7.5% when RisoP equals 50kΩ and RisoN is unlimited in room temperature.

2.3 Highlighted Products

2.3.1 BQ79731-Q1

The device can be used to measure divided down high-voltage nodes in a battery system. The device can measure voltage across fuses and contactors. The device can check isolation voltage in a battery junction box (BJB) system. The device has two integrated current sense (BQ79731-Q1) paths supporting low-side shunt resistors. The coulomb counting (BQ79731-Q1) function is available for accurate SOC calculation. There are 15 GPIOs and auxiliary inputs that can be used for high-voltage measurements, thermistor measurements, and driving relays. There are four software outputs that can be used to drive metal-oxide semiconductor field-effect transistor (MOSFET) switches in the measurement path. The device can function as an SPI hub and interface with up to eight separate SPI devices or groups. Overcurrent protection response can be achieved autonomously using hardware pins for fast protection in dangerous overcurrent events. The isolated bidirectional daisy chain ports support both capacitor and transformer-based isolation. The device can also communicate with the MCU over SPI.

2.3.2 TPSI2140-Q1

The TPSI2140-Q1 is an isolated solid-state relay designed for high-voltage automotive and industrial applications. The TPSI2140-Q1 uses TI's high-reliability capacitive isolation technology in combination with internal back-to-back MOSFETs to form a completely integrated design requiring no secondary-side power supply.

The primary side of the device is powered by only 9mA of input current and incorporates a fail-safe EN pin preventing any possibility of back-powering the VDD supply. In most applications, the VDD pin of the device must be connected to a system supply between 5V to 20V, and the EN pin of the device must be driven by a GPIO output with logic *high* between 2.1V to 20V. In other applications, the VDD and EN pins can be driven together directly from the system supply or from a GPIO output. All control configurations of the TPSI2140-Q1 do not require additional external components such as a resistor or low-side switch that are typically required in photo relay designs.

The secondary side consists of back-to-back MOSFETs with a standoff voltage of ±1.2kV from S1 to S2. The avalanche robustness of the TPSI2140-Q1 MOSFETs and thermally conscious package design allows robust support of system-level dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 2mA without requiring any external components.

2.3.3 ISO7841

The ISO7841x device is a high-performance, quad-channel digital isolator with a 8000V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, CQC, and TUV. The isolator provides high electromagnetic immunity and low-emissions at low-power consumption while isolating CMOS or LVCMOS digital inputs and outputs. Each isolation channel has a logic input and output buffer separated by a silicon-dioxide (SiO2) insulation barrier.

This device comes with enable pins that can be used to put the respective outputs in high-impedance for multi-controller driving applications and to reduce power consumption. The ISO7841 device has three forward and one reverse-direction channels. If the input power or signal is lost, the default output is high for the ISO7841 device and low for the ISO7841F device.

Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO7841 device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

The ISO7841 device is available in 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages.

2.3.4 SN6507

The SN6507 is a high-voltage, high-frequency push-pull transformer driver providing isolated power in a small design size. The device comes with the push-pull topology benefits of simplicity, low electromagnetic interference (EMI), and flux cancellation to prevent transformer saturation. Further space savings are achieved through duty-cycle control, which reduces component count for wide-input ranges, and by selecting a high switching frequency, reducing the size of the transformer.

The device integrates a controller and two 0.5A N-channel metal-oxide semiconductor (NMOS) power switches that switch out of phase. The input operating range is programmed with precision undervoltage lockouts. The device is protected from fault conditions by overcurrent protection (OCP), adjustable undervoltage lockout (UVLO), overvoltage lockout (OVLO), thermal shutdown (TSD), and break-before-make circuitry.

The programmable soft start minimizes inrush currents and provides power supply sequencing for critical power-up requirements. Spread spectrum clocking (SSC) and pin-configurable slew rate control (SRC) further reduces radiated and conducted emissions for ultra-low EMI requirements.

The SN6507 is available in a 10-pin HVSSOP DGQ package. The device operation is characterized for a temperature range from –55°C to 125°C.

2.3.5 TPS7B6950

The TPS7B69xx device is a low-dropout linear regulator that operates at up to 40V V_I with only 15µA (typical) quiescent current at light load. The device is applicable for standby micro control-unit systems, especially for always-on applications like e-meters, fire alarms, and smoke detectors.

The devices have integrated short-circuit and overcurrent protection. The TPS7B69xx device operates over a –40°C to 105°C temperature range.

3 Hardware, Software, Testing Requirements, and Test Results

The key performances of the TIDA-010272 were tested in a TI lab, and the end equipment used and test processes and results are described in this section.

Table 3-1 describes the connections for the TIDA-010272 board.

Table 3-1. Positive High-Voltage Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J24-1	N/A	N/A
J24-2	BATP	Positive terminal of battery
J24-3	RACKP	Positive terminal of rack

Table 3-2. Negative High-Voltage Battery Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J22-1	RACKN	Negative terminal of rack
J22-2	BATN	Negative terminal of battery
J22-3	N/A	N/A

Table 3-3. Host Interface

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J8-1	ISO_OC2_R	Isolated over current alarm from BQ79731 CSADC1
J8-3	ISO_SCLK	
J8-5	ISO_GND	
J8-7	ISO_MOSI_RX	Isolated MOSI/RX of BQ7973x
J8-9	ISO_nCS	
J8-2	ISO_nFAULT_OD	BQ7973x NFAULT pin
J8-4	ISO_OC1_R	Isolated overcurrent alarm from BQ79731 CSADC2
J8-6	USB2ANY_3.3V	Isolated USB2ANY 3.3V
J8-8	ISO_MISO_TX	Isolated MISO/TX of BQ7973x
J8-10	ISO_nUART_SPI	

Table 3-4. Current Sensor 1 Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J28-1	SRP1_RES	Current sensing positive terminal for channel 1
J28-2	SRN1_RES	Current sensing negative terminal for channel 1
J28-3	GND	GND of BQ7973x
J28-4	NTC1_RTN	Return pin of thermistor 1
J28-5	NTC1_SNS	Sensing pin of thermistor 1

Table 3-5. Current Sensor 2 Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J29-1	SRP2_RES	Current sensing positive terminal for channel 2
J29-2	SRN2_RES	Current sensing negative terminal for channel 2
J29-3	GND	GND of BQ7973x
J29-4	NTC2_RTN	Return pin of thermistor 2
J29-5	NTC2_SNS	Sensing pin of thermistor 2

Table 3-6. Daisy Chain (COML) Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J35-4	COMLP_ISO	COM low-side positive
J35-1	COMLN_ISO	COM low-side negative

Table 3-7. Daisy Chain (COMH) Connector

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J37-1	COMHP_ISO	COM high-side positive
J37-4	COMHN_ISO	COM high-side negative

Table 3-8. Low-Voltage Side Power Supply

CONNECTOR AND PIN ASSIGNMENTS	FUNCTION OR SCHEMATIC NET	NOTES
J1-1	KL30_IN	Positive terminal of 24V DC power supply
J1-2	GND_LV	Negative terminal of 24V DC power supply
J1-3	GND_LV	Negative terminal of 24V DC power supply

3.1 Hardware Requirements

Table 3-9 summarizes the equipment used for testing.

Table 3-9. Test Equipment Summary

EQUIPMENT	MODEL OR DESCRIPTION
Multimeter	Agilent® 34401A
Precise shunt simulator	JOY 7307
USB2ANY	TI HAP655

TI recommends the *Battery Management Studio (bqStudio) Software* when debugging the board for the first time.

3.2 Test Setup

Figure 3-1 shows the HMU test setup.

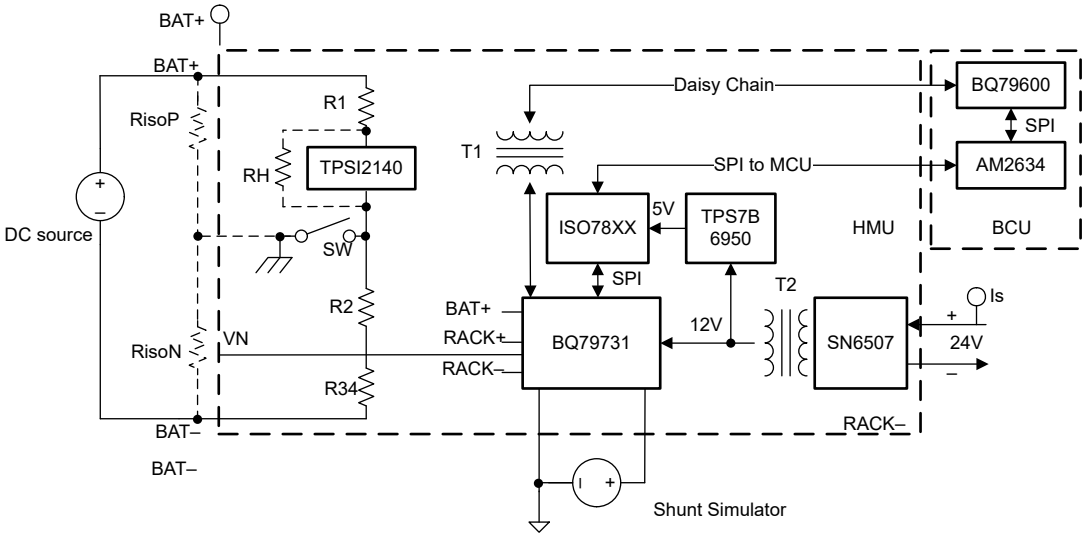


Figure 3-1. HMU Test Setup

Use the following procedures before running this design board. The design was constructed with a 1500V rack configuration. The board was tested using a high-voltage DC source to provide the total rack. The test points RACK– and BAT– are connected to the negative terminal of the DC source. The test point BAT+ is connected to the positive terminal of the DC source.

1. Connect the shunt simulator to the current sensing negative terminal (SRN) and current sensing positive terminal (SRP) of CSADC1
2. Use 50kΩ and 10MΩ high-voltage resistors as RisoP and RisoN

3.3 Test Results

3.3.1 Bus Voltage Accuracy

The test setup follows Figure 3-1. This design measures the VBAT channel in the board connected to the 1500V DC source. The source is set as 500V to 1500V and the working voltage of ESS is assumed to be 1100V to 1500V. VF1_7 is the BQ79731 reading data. VBAT_7 is the VBAT voltage calculated by BQ79731. VBAT_7 equals Ratio multiplied by VF1_7. The ratio is the voltage gain which equals 361.7214429 in this design. The calibration process uses test points of 1100V and 1500V to remove the offset error caused by BQ79731 VF1 ADC and gain error caused by resistor error.

Table 3-10 shows the bus voltage accuracy data measured by BQ79731 VF1. The ladder and sensing resistors of BAT voltage have 1% accuracy. The accuracy before calibration is 0.76% maximum. After calibration, the accuracy is less than 0.1% when the bus voltage ≥ 500V, and a maximum 0.3V absolute error when the bus voltage is 500V. This easily meets the requirement in GBT34131-2023 as 0.5% when the bus voltage is ≥ 500V and 5V when the bus voltage is < 500V.

Table 3-10. Bus Voltage Accuracy Data

VF1_7 (V)	METER READINGS VBAT_M (V)	BEFORE CALIBRATION		AFTER CALIBRATION	
		VBAT_7 (V)	ACCURACY	VBAT_7_c (V)	ACCURACY
1.3894	499.898	502.5758	0.53%	500.2247	0.07% (Abs 0.3V)
2.225	799.881	804.8302	0.61%	799.7497	–0.02%
2.7834	999.868	1006.815	0.69%	999.911	0.00%
3.0624	1099.92	1107.736	0.71%	1099.92	0.00%
3.6197	1299.92	1309.323	0.72%	1299.687	–0.02%
4.1783	1499.92	1511.381	0.76%	1499.92	0.00%

Figure 3-2 shows the bus voltage accuracy curve measured with BQ79731 VF1.

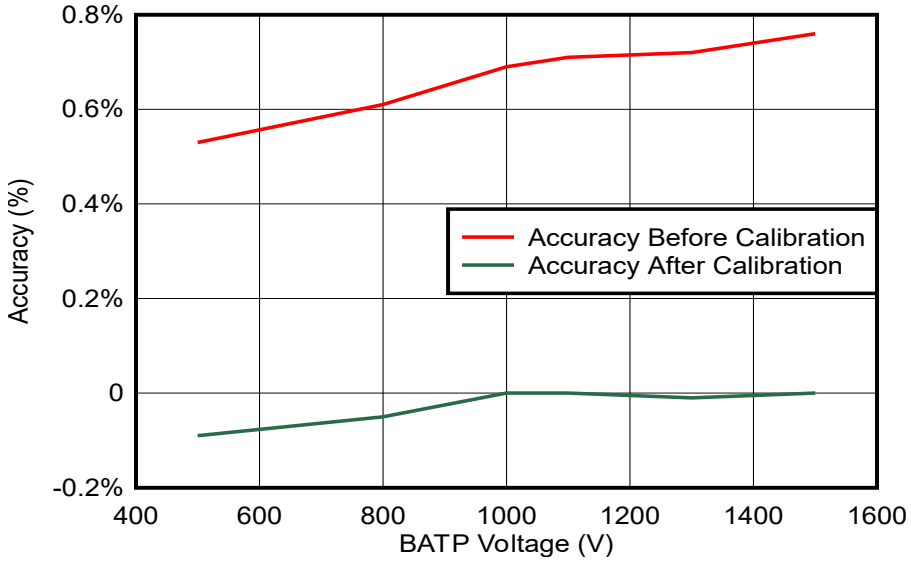


Figure 3-2. Bus Voltage Accuracy Curve

3.3.2 Current Sensing Accuracy

The test setup follows Figure 3-1. A high-precision voltage source provides eleven voltage test points from –75mV to 75mV to simulate shunt current range from –500A to 500A in a 150μΩ shunt. To verify the current resolution of the current sensing circuit, 1500μV (10A across the 150μΩ shunt) is applied.

Table 3-11 shows the current sensing accuracy data measured with BQ79731 CSADC1. The maximum error before calibration is 58.79μV. The maximum error after calibration is 9.87μV. Assuming the shunt resistance is 150μΩ, after calibration, the current accuracy is less than 0.007% when shunt current > 10A, and maximum 6.56mA absolute error when shunt current ≤ 10A.

Table 3-11. Current Sensing Accuracy Data

	CSADC1 ACCURACY BEFORE CALIBRATION		CSADC1 ACCURACY AFTER CALIBRATION		SHUNT CURRENT SENSING ACCURACY AFTER CALIBRATION		
Simulator_ voltage (μV)	CSADC1_ Reading_ uncal (μV)	CSADC1_ uncal_ error (μV)	CSADC1_ reading_cal (μV)	CSADC1_cal_ error (μV)	Error (%)	150μΩ SHUNT CURRENT ERROR (mA)	150μΩ SHUNT CURRENT (A)
–75000	–74941.21	58.79	–74990.13	9.87	–0.0001	65.82	–500.00
–2500	–2490.96	9.04	–2501.08	–1.08	0.0004	–7.20	–16.67
–1500	–1491.40	8.60	–1500.98	–0.98	0.0007	–6.56	–10.00
–250	–242.07	7.93	–250.99	–0.99	0.0039	–6.58	–1.67
–150	–142.01	7.99	–150.87	–0.87	0.0058	–5.77	–1.00
0	8.78	8.78	0.00	0.00	NA	0.03	0.00
150	159.25	9.25	150.56	0.56	0.0037	3.70	1.00
250	259.37	9.37	250.73	0.73	0.0029	4.85	1.67
1500	1507.90	7.90	1499.92	–0.08	–0.0001	–0.52	10.00
2500	2507.21	7.21	2499.77	–0.23	–0.0001	–1.54	16.67
75000	74968.64	–31.36	75000.00	0.00	0.0000	0.03	500.00

Figure 3-3 shows the shunt voltage accuracy curve measured with BQ79731 CSADC1.

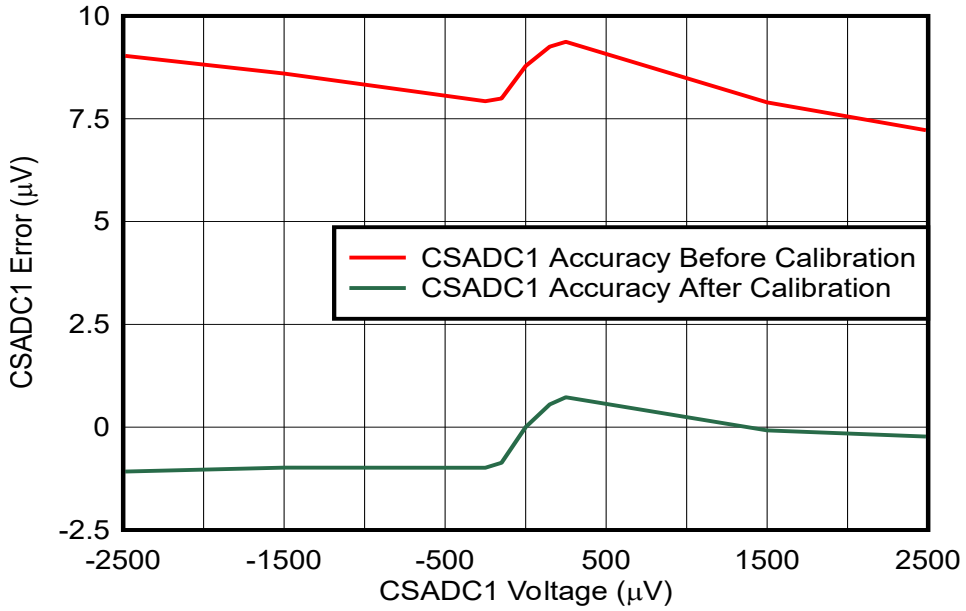


Figure 3-3. CSADC1 Accuracy Curve

3.3.3 Insulation Impedance Accuracy

The test setup follows Figure 3-1. A high-voltage DC source provides 1500V to simulate a rack. To verify the current accuracy of the current-sensing circuit, 1500µV (10mA across the 150µΩ shunt) is applied.

Table 3-12 shows the insulation impedance accuracy data. The maximum error of RisoP and RisoN is 6.32% and 3kΩ when RisoP is 50kΩ and RisoN is not connected.

Table 3-12. Insulation Impedance Accuracy Data

RisoP (kΩ)	RisoN (kΩ)	ERROR OF RisoP	ERROR OF RisoN
50	Not connected	6.32% (3kΩ)	NA
50	50	–0.83%	–1.15%
10000	Not connected	–0.67%	NA
10000	10000	–0.65%	–0.28%
Not connected	50	NA	–1.54%
Not connected	10000	NA	–0.27%

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010272.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010272.

4.2 Tools and Software

Tools

USB2ANY Evaluation board	The USB2ANY interface adapter is a tool intended to allow a computer to control an evaluation module (EVM) via a USB connection. USB2ANY supports multiple popular protocol interfaces and provides 3.3V and 5V power supplies.

Software

BQSTUDIO	Battery Management Studio (bqStudio) Software
CCSTUDIO	Code Composer Studio™ integrated development environment (IDE)

4.3 Documentation Support

1. Texas Instruments, *LiFePO4 Design Considerations Application Note*
2. Texas Instruments, *Scaling accurate battery management designs across energy storage systems application brief*
3. Texas Instruments, *How to Stack Battery Monitors for High-Cell-Count Industrial Applications Technical Article*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

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