Design Guide: TIDA-050059

Overcurrent and Overtemperature Protection for Solid-State Relays Reference Design

Description

This reference design shows how to achieve overcurrent and overtemperature protection for a solid-state relay. The reference design features the TPSI3050-Q1 5 kV_{RMS} reinforced isolated switch driver. TPSI3050-Q1 device integrates a laminate transformer to achieve isolation while transferring signal and power to the secondary side. This removes the need for any isolated bias supply. In addition, the TPSI3050-Q1 device can supply power to external circuitry located on the high voltage (HV) side. This reference design can support up to 500 VDC or 350 VAC switching with a max of 4 A loading conditions.

Resources

TIDA-050059	Design Folder
TPSI3050-Q1, AMC23C14	Product Folder
SN74HCS09, TMP392	Product Folder
ISO7310-Q1	Product Folder

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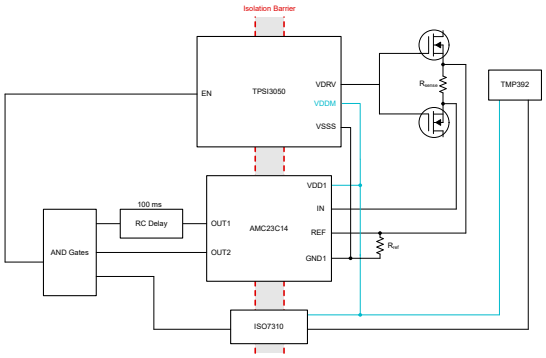
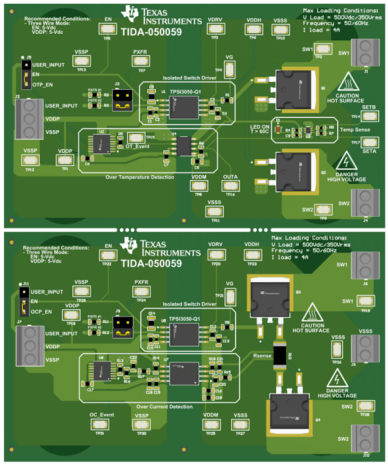
Features

- No need for isolated bias supply
- 3-kV_{RMS} reinforced isolation
- 500-V_{DC}/350-V_{RMS} load with 4-A max
- Two-level overcurrent protection
  - > 2-A 100-ms load disconnect delay
  - > 5-A immediate load disconnect
- Two-level overtemperature protection
  - > 60 °C LED visual warning
  - > 90 °C immediate load disconnect

Applications

- Solid State Relay (SSR)
- Hybrid, Electric, and Powertrain Systems
- Grid Infrastructure
- Building Automation
- Factory Automation and Control
- Appliances





1 System Description

This reference design shows how to achieve a solid state relay solution with overcurrent and overtemperature protection, using the reinforced isolated switch driver TPSI3050-Q1. Protecting sensitive circuit components from overstress conditions increases the lifetime of the overall system and reliability. The risks of not implementing a well-designed protection scheme can be catastrophic for the circuit in the presence of an overcurrent event. This reference design proposes a two-level overcurrent and overtemperature protection scheme.

For the overcurrent protection, a two-level protection scheme is designed such that when the current load is greater than 2 A but less than 5 A, the circuit logic provides a delay of at least 100 ms before the load is disconnected. This delay can be used to allow for momentary inrush currents in the case of a highly capacitive load. When the current load exceeds the the max limit of 5 A, the load is immediately disconnected. The immediate load disconnect is used in case of a dangerous short circuit.

In the case of the overtemperature protection, when the circuit is within the lower limit between 60 °C to 90 °C, a visual warning is shown by a red LED which represents a hot surface. When the temperature is above the upper limit 90 °C, the load is disconnected.

There are several advantages of using the TPSI3050-Q1 as an isolated switch driver. TPSI3050-Q1 eliminates the need for isolated bias and isolated supply by generating a well-regulated 10 V gate drive voltage and a 5 V supply to power the auxiliary circuit. In addition, TPSI3050-Q1 can supply up to 50 mW to auxiliary circuitry. The TPSI3050-Q1 offers 5 kV_{RMS} reinforced isolation and AEC-Q100 qualification for automotive applications while the TPSI3050 offers 3 kV_{RMS} basic isolation for industrial applications.

2 System Overview

2.1 Block Diagram

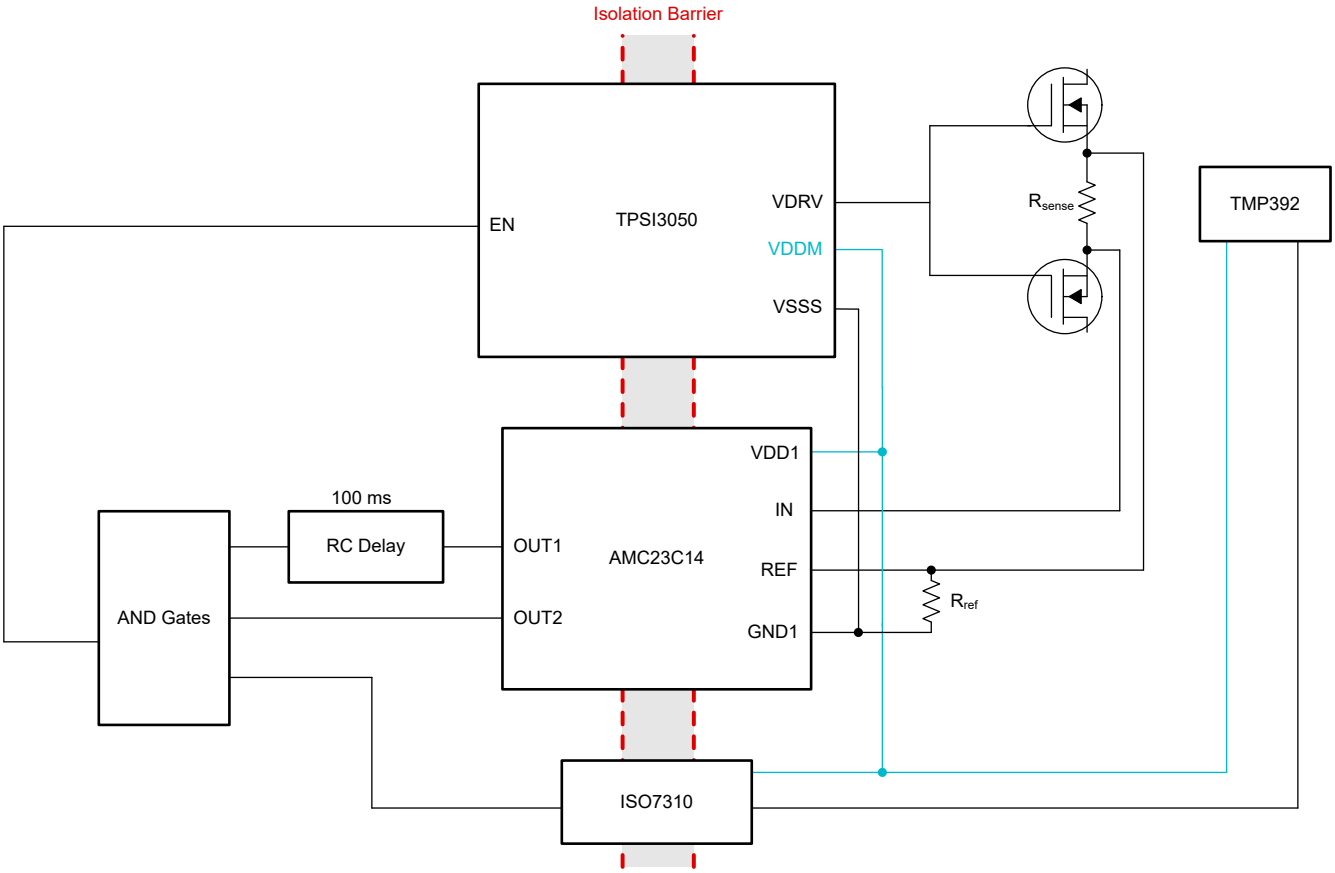


Figure 2-1. Block Diagram

2.2 Highlighted Products

The reference design features the TPSI3050-Q1, AMC23C14, SN74HCS09, TMP392, and ISO7310-Q1.

2.3 Design Considerations

The TPSI3050-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated solid-state relay (SSR) solution. With a nominal gate drive voltage of 10 V and 1.5/3.0 A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3050-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required. Additionally, the TPSI3050-Q1 can optionally supply power to external supporting circuitry for various application needs. In three-wire mode, the primary supply of 3 V to 5.5 V is supplied externally, and the switch is controlled through a separate enable.

TPSI3050-Q1 features:

- Adjustable power transfer
- Integrated 10-V gate supply
- Up to 50 mW supply to power auxiliary circuitry (I_{AUX})

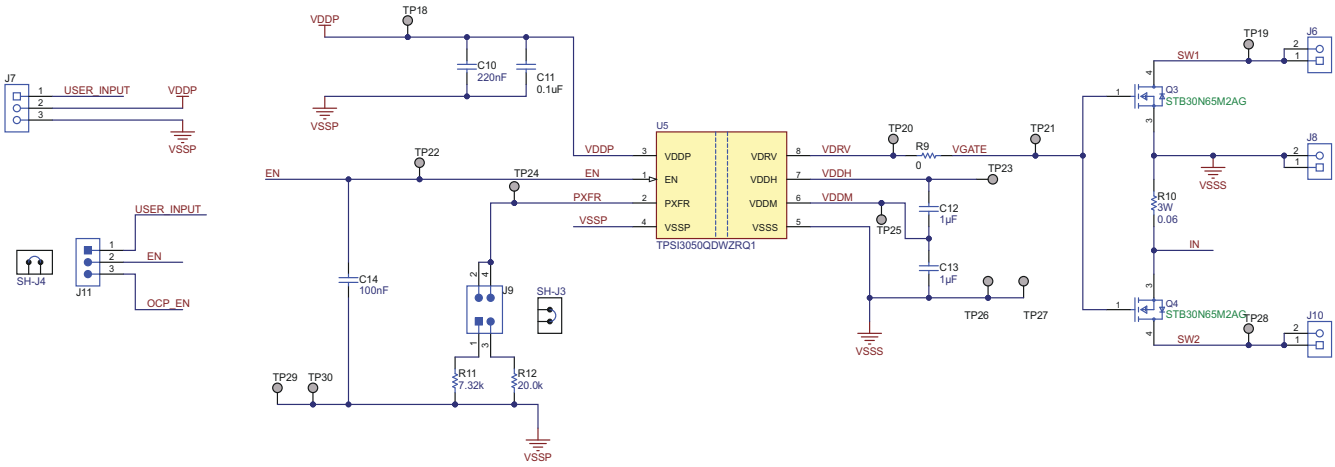


Figure 2-2. Solid-State Relay Circuit

For the primary side, TPSI3050-Q1 is set to three-wire mode configuration to achieve the highest power transfer available. Using a 20 kΩ resistor with a 1 % tolerance in PXFR pin provides the highest power transfer available and supports up to 50 mW of I_{AUX}. It is recommended to add a 1 uF in parallel with a 0.1 uF ceramic capacitor with low ESR to VDDP.

For the secondary side, C_{DIV1} (C12) and C_{DIV2} (C13) capacitors need to be properly selected to drive the back to back MOSFETs. If C_{DIV1} and C_{DIV2} are too small, then the voltage drop in VDDH will trigger an undervoltage lockout (UVLO) and disable the driver. The following two equations can be used for calculating the proper capacitance values.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V}, \quad n \geq 1.0 \tag{1}$$

$$C_{DIV2} = n \times C_{DIV1}, \quad n \geq 1.0 \tag{2}$$

- n is a real number greater than or equal to 1.0.
- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

The MOSFETs selected for this design each have a gate charge (Q_G) of 31 nC. Since the design uses back to back MOSFETs, then the total Q_G is 62 nC. If C_{DIV1} = C_{DIV2}= C_{DIV}, then C_{DIV} must be selected with capacitance higher than 124 nF to ensure that VDDH voltage drop is less than 1 V. Use this excel calculator to calculate for capacitors and power transfer selection. For this design a 1 uF capacitor was selected to have a VDDH voltage drop of 0.124 V.

2.3.1 Overcurrent Protection (OCP)

The AMC23C14 is a dual, isolated window comparator with a short response time. The opendrain outputs are separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to UL1577, and supports a working voltage of up to 1 kV_{PK}.

Both comparators have windows that are centered around 0 V, meaning that the comparators trip if the input exceeds the thresholds in a positive or negative direction. One comparator has fixed thresholds of ±300 mV. The second comparator has adjustable thresholds from ±20 mV to ±300 mV through a single external resistor.

AMC23C14 features:

- Wide high-side supply range: 3 V to 27 V
- Low-side supply range: 2.7 V to 5.5 V
- Dual window comparator:
  - Window comparator 1: ±20 mV to ±300 mV adjustable threshold
  - Window comparator 2: ±300 mV fixed threshold
- Propagation delay: 290 ns (typ)
- High CMTI: 15 kV/µs (min)
- Open-drain outputs

For VDD1 and VDD2, it is recommended to add a low-ESR, 100-nF capacitor parallel to a low-ESR, 1-µF capacitor. AMC23C14 is powered on the HV side by TPSI3050-Q1 from the VDDM pin with a 5 V rail. This feature of TPSI3050-Q1 reduces system complexity, cost, and board space.

AMC23C14 is a dual window comparator that can be used for a two-level overcurrent protection. In many applications, the system needs to support inrush currents when initially connected to the load. Using a two level implementation can allow for large inrush currents for a very short period of time and protect the system in the case of short circuit event. This reference design uses the adjustable threshold of the second comparator to allow for currents between 2 A to 5 A for at least 100 ms. If the inrush current remains for more than 100 ms, then the load is diconnected. This delay of 100 ms is accomplished with a simple RC time constant. However, if the overcurrent exceeds 5 A, then the load is disconnected immediately. The immediate load disconnect is accomplished using the fixed threshold from the first comparator. The following sections explain the design of the two level protection in details.

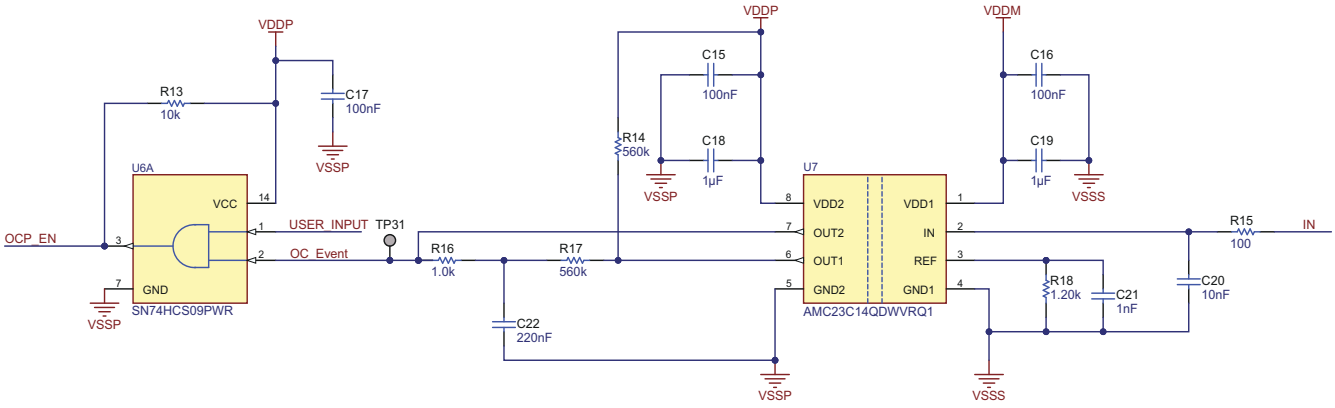


Figure 2-3. Overcurrent Detection Circuit

2.3.1.1 Immediate Overcurrent Protection

When the system experiences a large overcurrent greater than 5 A, the overcurrent protection disconnects the load immediately. The sense resistor (R10) is selected to create a voltage drop of 300 mV at expected current limit. For this design a 5 A is the selected current limit threshold. When the current is higher than 5 A, OUT2 changes state from High-Z to Low-Z. Equation 3 shows the calculation for the sense resistor value.

$$R_{sense} = \frac{V_{TRIP\_FIXED}}{I_{FAULT}} = \frac{300\ mV}{5\ A} = 60\ m\Omega \quad (3)$$

The power rating of the shunt should be at least 30% higher than the peak power dissipation as a recommended design margin. The tolerance of the resistor should be 1% or less to allow for higher overcurrent protection accuracy. Equation 4 provides the calculation for the peak power dissipation across the sense resistor. For this design a resistor with a 3 W capability was selected for design margin.

$$P_{max} = i^2 \times R_{SENSE} = 1.5\ W \quad (4)$$

Figure 2-4 shows a detailed analysis of the charging and discharging paths. When the current load (ILOAD) through R10 is higher than 5 A, a voltage drop of 300 mV is created in R10. OUT2 is pulled to ground when the voltage drop is greater than 300 mV. When OUT2 is Low-Z, the input of the AND gate (SN74HCS09) is immediately pulled to ground, the output of the AND gate (EN) is asserted low and the load is disconnected. Discharge Path 2 in Figure 2-4 shows how C22 is discharged when OUT2 is pulled low. R16 is placed to limit the inrush current from C22 through OUT2. Since OUT1 and OUT2 are pulled low, C22 discharges below the negative switching threshold (V_{T-}) of the AND gate in 180-us as the following equation shows. Note that the following equation only accounts for Discharging Path 2 for simplicity.

$$t_{discharge} = -R16 \times C22 \times \ln\left(\frac{VC22}{V_{SOURCE}}\right) \quad (5)$$

$$t_{discharge} = -1\ k\Omega \times 220\ nF \times \ln\left(\frac{2.2\ V}{5\ V}\right) = 180.62\ \mu s$$

When the load is disconnected, the circuit attempts to reconnect the load automatically. When the voltage across the capacitor is charged above the positive switching threshold (V_{T+}) of the AND gate, then EN is asserted high and the load connected. The AND gate (SN74HCS09) guarantees by design a minimum hysteresis of 0.4 V (V_{HYS}). With this hysteresis value, the following equations shows that at least 38 ms will passed before the load is reconnected.

$$t_{charge} = -(R14 + R17) \times C22 \times \ln\left(\frac{V_{SOURCE} - (V_{INITIAL} + V_{HYS})}{V_{SOURCE} - V_{INITIAL}}\right) \quad (6)$$

$$t_{charge} = -\left(560\ k\Omega + 560\ k\Omega\right) \times 220\ nF \times \ln\left(\frac{5\ V - 2.2\ V - 0.4\ V}{5\ V - 2.2\ V}\right) = 37.98\ ms$$

2.3.1.2 Adjustable Delay Overcurrent Protection

In some cases, it might be preferable to allow an overcurrent condition for a certain period of time. A example of this could be a highly capacitive circuit in which a temporary inrush current is allowed to charge the capacitor. AMC23C14 has an adjustable threshold which is created through a current source of 100 uA and a reference resistor. Equation 7 and Equation 8 show how to calculate for the reference resistor (R_{REF}). This range is used to allow for 100-ms of inrush currents between 2 A to 5 A. For this reference design a typical resistor of 1.2 kΩ was selected.

$$V_{TRIP} = I_{MAX} \times R_{SENSE} = 2\ A \times 60\ m\Omega = 120\ mV \quad (7)$$

$$R_{REF} = \frac{V_{TRIP} - V_{HYS}}{I_{REF}} = \frac{120\ mV - 4\ mV}{100\ \mu A} = 1.16\ k\Omega \quad (8)$$

Discharging Path 1 in Figure 2-4 shows that when the system is operating under normal conditions (current load less than 2 A), OUT1 is High-Z and C22 is charged to 5 V (VDD2). When the current is greater than 2 A, OUT1 is Low-Z and C22 begins to discharge through R17. The time to discharge C22 should be at least 100 ms before reaching the maximum switching threshold for SN74HCS09 of 2.2 V as shown in Equation 9.

$$t_{discharge} = -R17 \times C22 \times \ln\left(\frac{VC22}{V_{SOURCE}}\right) \quad (9)$$

$$t_{discharge} = -560\ k\Omega \times 220\ nF \times \ln\left(\frac{2.2\ V}{5\ V}\right) = 101.15\ ms$$

When the load is disconnected, the circuit attempts to reconnect the load automatically. When the voltage across the capacitor is charged above the positive switching threshold (V_{T+}) of the AND gate, then EN is asserted high and the load connected. The AND gate (SN74HCS09) guarantees by design a minimum hysteresis of 0.4 V. With this hysteresis value, the following equations shows that at least 38 ms will passed before the load is reconnected. Is it important to select R14 to allow for a large charging time for C22 for the system not to reconnect the load immediately.

$$t_{charge} = -(R14 + R17) \times C22 \times \ln\left(\frac{V_{SOURCE} - (V_{INITIAL} + V_{HYS})}{V_{SOURCE} - V_{INITIAL}}\right) \quad (10)$$

$$t_{charge} = -\left(560\ k\Omega + 560\ k\Omega\right) \times 220\ nF \times \ln\left(\frac{5\ V - 2.2\ V - 0.4\ V}{5\ V - 2.2\ V}\right) = 37.98\ ms$$

It is recommended to add R15 and C20 to filter any high frequency noises. High frequency noises can disturb the behavior of the isolated comparator.

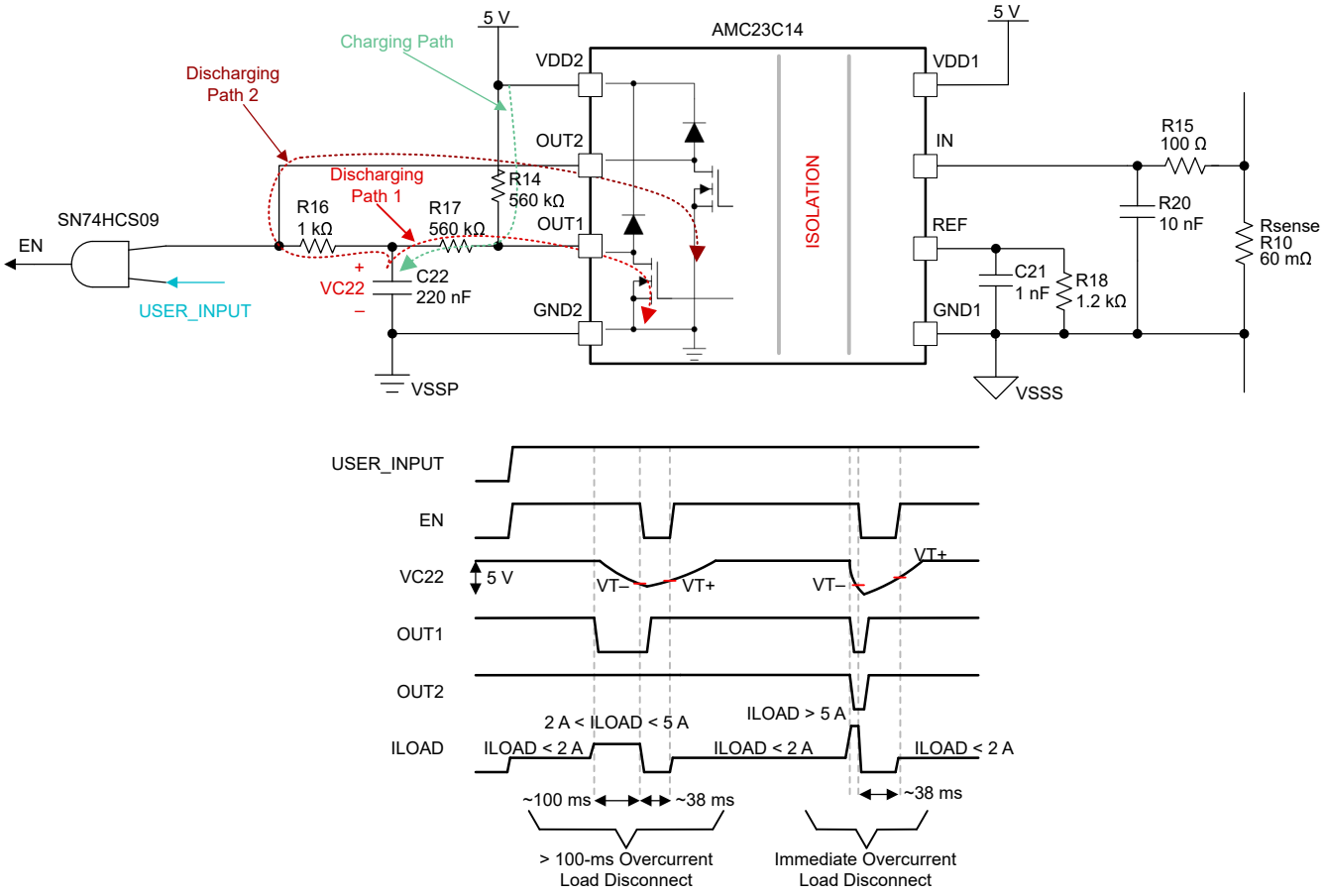


Figure 2-4. Overcurrent Protection

2.3.2 Overtemperature Protection (OTP)

2.3.2.1 TMP392

The TMP392 device is part of a family of ultra-low power, dual channel, resistor programmable temperature switches that enable protection and detection of system thermal events from 30 °C to 130 °C. The TMP392 offers dual overtemperature (hot and warm) detection. The trip temperatures (T_{TRIP}) and thermal hysteresis (T_{HYST}) options are programmed by two E96-series resistors (1 % tolerance) on the SETA and SETB pins. Channel A resistors can range from 1.05 kΩ to 909 kΩ, representing one of 48 unique values. Channel B resistors can range from 10.5 kΩ to 909 kΩ.

The value of the resistor to ground on SETA input sets the T_{TRIP} threshold of Channel A. The value of the resistor to ground on SETB input sets the T_{TRIP} threshold of Channel B, as well as the T_{HYST} options of 5 °C, or 1 °C for both channels, to prevent undesired digital output switching. When the SETB input is connected to ground, Channel A operates with 20 °C hysteresis.

TMP392 Features:

- Resistor programmable temperature trip points
- Dual output selection
- Ultra-low power consumption
- Open-drain outputs

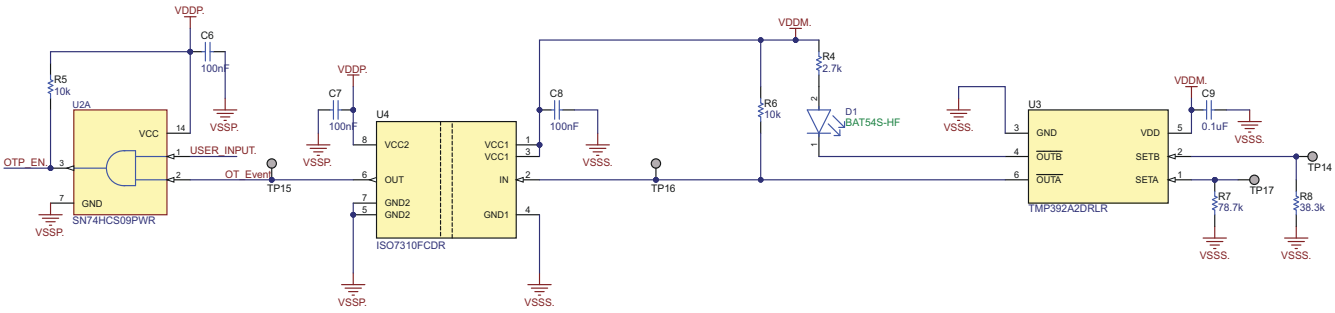


Figure 2-5. Overtemperature Detection Circuit

For this design, the dual overtemperature protection was selected such that when temperature is between 60 °C to 90 °C, a visual warning is provided via a red LED. The LED selected for this design is LSL29K-G1H2-1-Z which only requires 2 mA to provide high luminous intensity. TPSI3050-Q1 can provide a max of 50 mW of power that must be carefully distributed for the auxiliary circuitry. When the temperature is higher than 90 °C the circuit immediately disconnects the load. The Channel A (HOT) temperature is set to trip at 90 °C by the 78.7 kΩ resistor between SETA and ground while Channel B (WARM) is set to trip at 60 °C by the 38.3 kΩ resistor connected between SETB and ground. The 38.3 kΩ resistor on SETB also set the hysteresis for both channels to 5 °C.

2.3.2.2 ISO7310

ISO7310 transfers signal to low voltage side as the input to the AND gate. The ISO7310-Q1 device provides galvanic isolation up to 3000 V_{RMS} for 1 minute per UL 1577 and 4242 V_{PK} per VDE V 0884-10. These devices have one isolated channel comprised of a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, the ISO7310-Q1 device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The device has integrated noise filters for harsh industrial environment where short noise pulses might be present at the device input pins.

The ISO7310-Q1 device has TTL input thresholds and operates from 3 V to 5.5 V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO7310-Q1 device has been significantly enhanced to enable system-level ESD, EFT, Surge and Emissions compliance.

The digital isolator is used to transfer the signal to the low voltage side as the input to SN74HCS09 AND gate to assert EN high when the user provides a high signal for EN.

3 Hardware, Software, Testing Requirements, and Test Results

For a functionality test of the reference design the user needs the following devices.

1. 5-V DC power source
2. Oscilloscope
3. Isolated probes
4. AC/DC power source
5. Load resistor

3.1 Hardware Requirements

3.2 Test Setup

To test the overcurrent protection reference design it is recommended to connect an oscilloscope to EN (enable), OC Event (output of the isolated comparator AMC23C14), and a differential probe to the AC source. Connect a 5 V power source and ensure that the TPSI3050-Q1 has powered up by measuring VDDH (10 V) and VDDM (5 V). Finally, connect the AC or DC source and the load to test the design.

To test the overtemperature protection reference design it is recommended to connect an oscilloscope to EN (enable), OT Event (output of the digital isolator), and a differential probe to the AC source. Connect a 5 V power source and ensure that the TPSI3050-Q1 has powered up by measuring VDDH (10 V) and VDDM (5 V). Finally, connect the AC or DC source and the load to tests the design.

The circuit should look as Figure 3-1.

Table 3-1. Test Points and Connectors

Name		Description
J1, J6, TP2, TP19	SW1	AC/DC source connection
J2, J7	USER_INPUT	External signal to control TPSI3050-Q1 EN signal
	VDDP	Power supply for primary side
	VSSP	Ground supply for primary side
J3, J9		Power transfer selection
J4, J10, TP9, TP28	SW2	Load connection
J5	USER_INPUT	External signal to control TPSI3050-Q1 EN signal without overtemperature protection
	EN	TPSI3050-Q1 Active high driver enable
	OTP_EN	Overtemperature enable signal to control TPSI3050-Q1
J11	USER_INPUT	External signal to control TPSI3050-Q1 EN signal without overcurrent protection
	EN	TPSI3050-Q1 Active high driver enable
	OCP_EN	Overcurrent enable signal to control TPSI3050-Q1
TP1, TP18	VDDP	TPSI3050-Q1 Power supply for primary side
TP3, TP20	VDRV	TPSI3050-Q1 Active high driver output
TP4, TP21	VG	Gate voltage of the power switches
TP5, TP22	EN	TPSI3050-Q1 Active high driver enable
TP6, TP23	VDDH	TPSI3050-Q1 Generated high supply
TP7, TP24	PXFR	TPSI3050-Q1 Increase or decrease power transfer
TP8, TP25	VDDM	TPSI3050-Q1 Generated mid supply
J8, TP10, TP11, TP26, TP27	VSSS	Ground supply for secondary side
TP12, TP13, TP29, TP30	VSSP	Ground supply for primary side
TP14	SETB	Temperature sensor debug input

Table 3-1. Test Points and Connectors (continued)

Name		Description
TP15	OT_EVENT	Active high signal that is pull down when overtemperature event above 90 °C occurs.
TP16	OUTA	Output of the temperature sensor
TP17	SETA	Temperature sensor debug input
TP31	OC_EVENT	Active high signal that is pull down when overcurrent event above 2 A occurs.

Steps to Test the Reference Design:

1. J3/J9 Connector should be connecting R3 (20 kΩ). This allows for the highest power transfer.
2. J5/J11 Connector should be connecting OTP_EN/OCP_EN to EN. This allows the TPSI3050-Q1 to be controlled by the overtemperature/overcurrent detection logic.
3. Connect 5-V supply to VDDP.
4. Check that VDDM and VDDH rails are 5-V and 10-V respectively.
5. Connect DC source with a load.
6. Connect 5-V supply to USER_INPUT

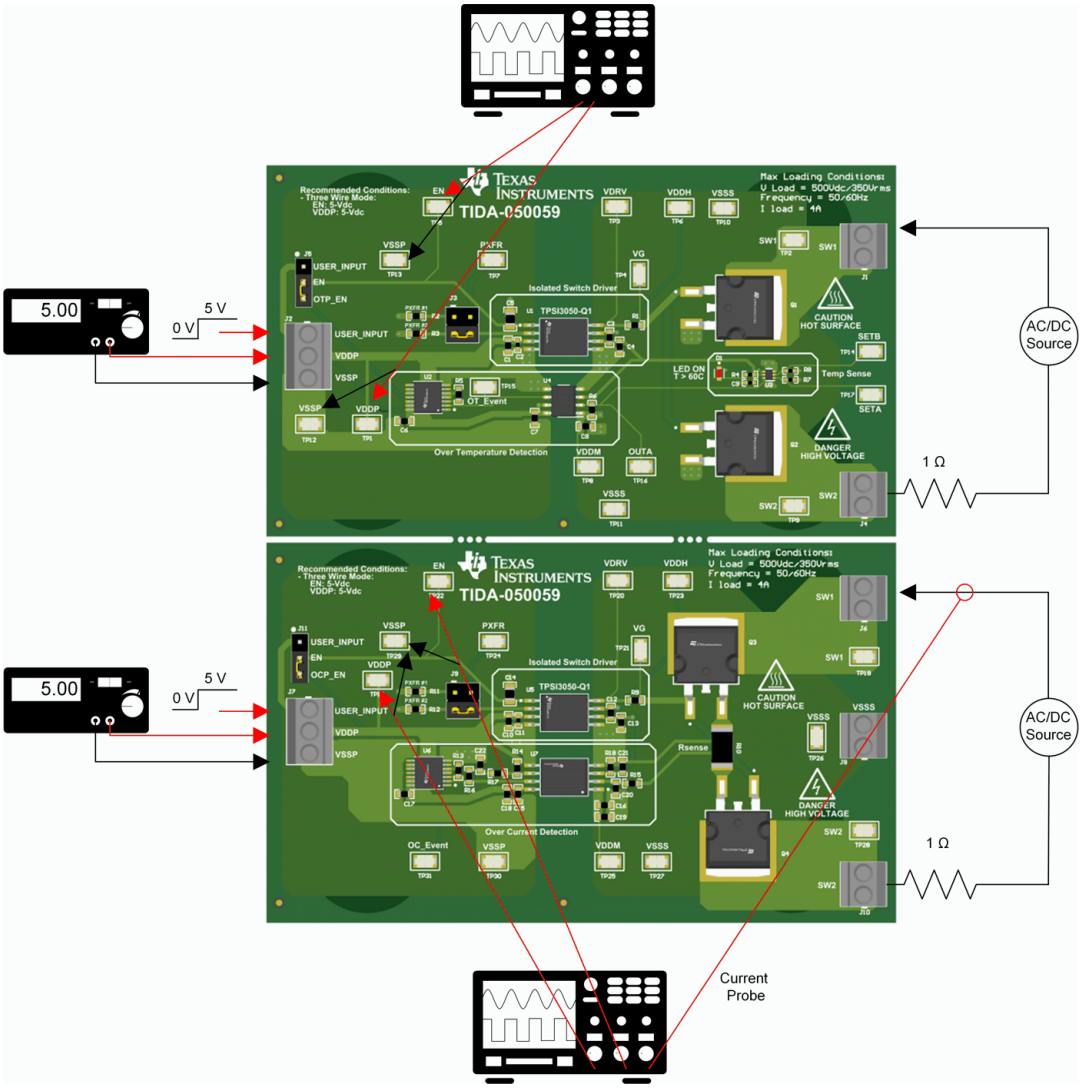


Figure 3-1. Test Setup

3.3 Test Results

Figure 3-2 shows when the load current (ILOAD) is greater or equal to 2 A and the design implements a delay of at least 100 ms before disconnecting the load. From the scope capture taken, it can be observed that the delay is larger than 100 ms. This is because the negative swing threshold from the AND gate can vary from 0.9 V to 2.2 V. The max value of 2.2 V was chosen for the calculation to ensure that the delay is greater or equal to 100 ms.

- VDDP is the power supply for primary side.
- USER_INPUT is the input provided by the user when desired to connect the load.
- EN is the enable input to TPSI3050-Q1.
- ILOAD is the current through the load.

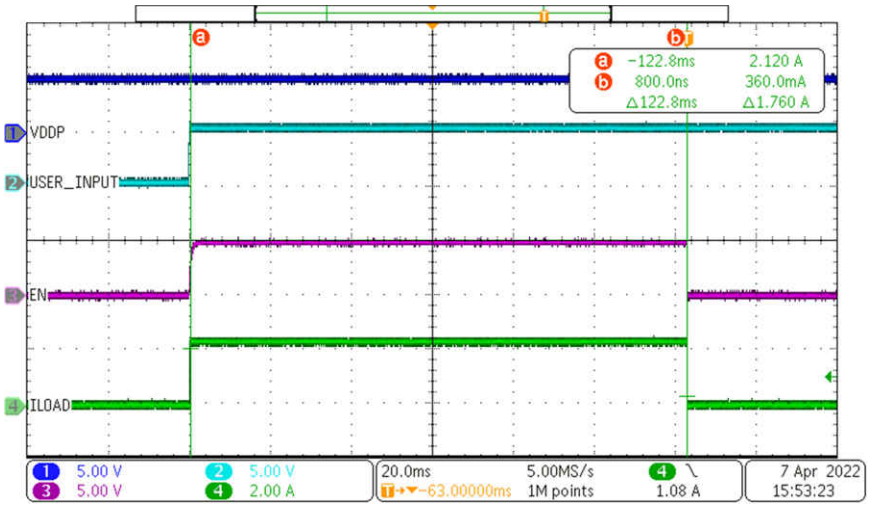


Figure 3-2. Scope Capture for 100-ms Delay Load Disconnect

Figure 3-3 shows the behavior of the circuit when a current greater than 5 A is detected. The current load increases above 5 A and the overcurrent protection disconnects the load with a minimal propagation delay of 6.3 µs.

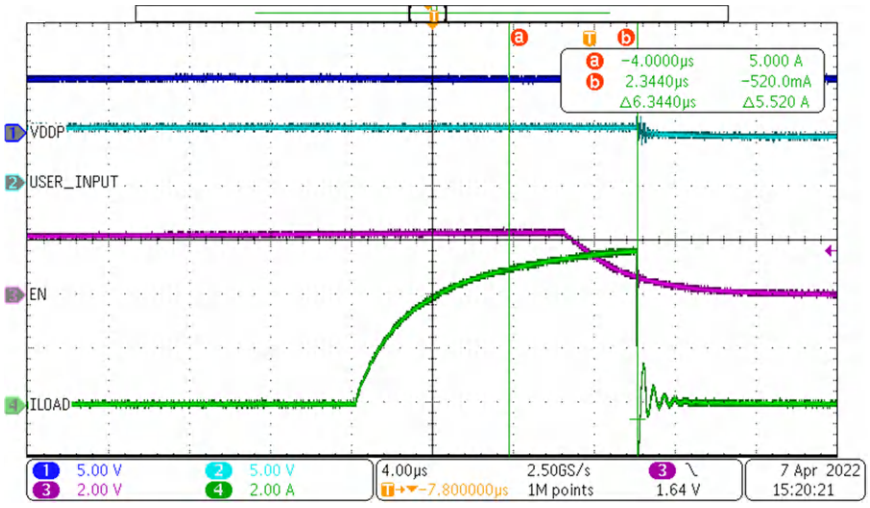


Figure 3-3. Scope Capture for Immediate Load Disconnect

Figure 3-4 shows the visual warning using a red LED when the temperature reaches 60 °C. Figure 3-5 and Figure 3-6 are thermal images taken for the two temperature protection levels. When temperature is between 60 °C to 90 °C a visual warning is provided via a red LED and when temperature is above 90 °C the load is disconnected.

Figure 3-4. Red LED Warning Light

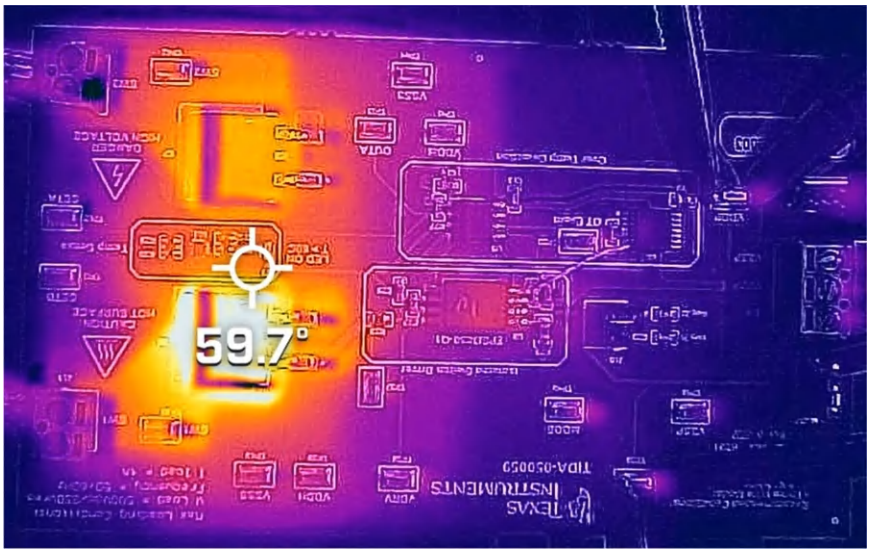


Figure 3-5. Thermal Image

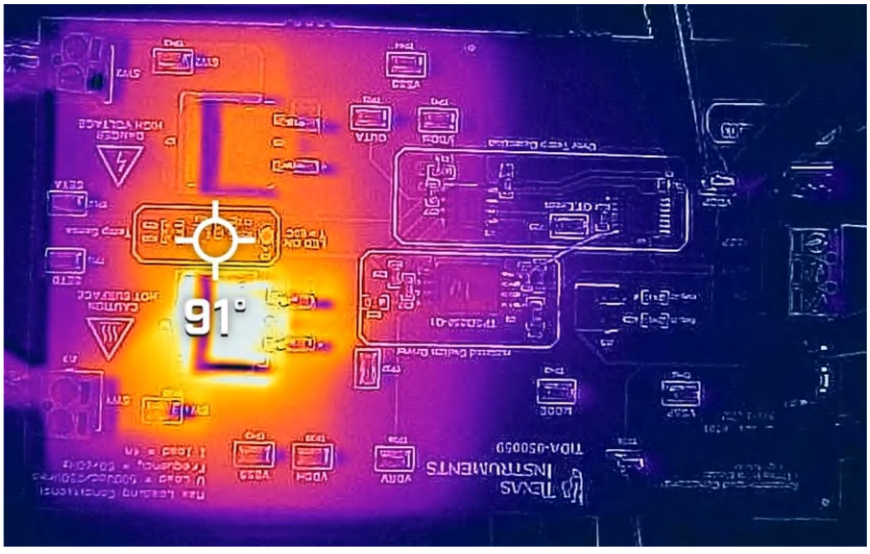


Figure 3-6. Thermal Image

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050059.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050059.

4.1.3 Altium Project

To download the Altium Designer™ project files, see the design files at TIDA-050059.

4.1.4 Assembly Drawings

To download the assembly drawings files, see the design files at TIDA-050059.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050059.

4.2 Documentation Support

1. Texas Instruments, TPSI3050-Q1 EVM Automotive Reinforced Isolated Switch Driver with Integrated 10-V Gate Supply EVM User's Guide user's guide.
2. Texas Instruments, AMC23C14 EVM Isolated Comparator Evaluation Module user's guide.
3. Texas Instruments, Cascoding Two TPSI3050 Isolated Switch Drivers to Increase Gate Drive Voltage application note.
4. Texas Instruments, TMP392 EVM user's guide.
5. Texas Instruments, ISO7310-Q1 EVM Universal Digital Isolator Evaluation Module user's guide.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

Alex Triano is the Product Marketing and Applications Manager of Texas Instruments Solid State Relay business, where he is responsible for defining and developing the next-generation of solid state relay solutions using capacitive and inductive isolation technologies. With a background in analog power, Alex joined TI in 2013 as part of the Power Interface business upon completion of his undergraduate studies at Stony Brook University. He served as an applications engineer, supporting customers worldwide with their power designs and helped solve complex issues requiring system-level analysis and debug. He has shared his knowledge throughout blogs, videos, and application notes to educate customers about these products and make the products easier to design with.

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