EVM User's Guide: AUDIO-AM275-EVM AUDIO-AM62D-EVM

DP83867-EVM-AM User Guide

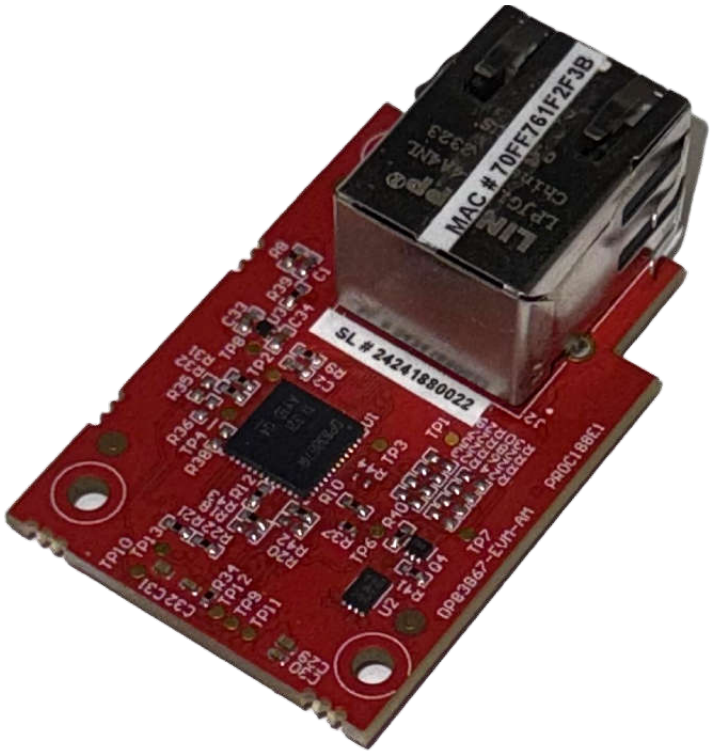
Description

DP83867-EVM-AM is an Industrial Ethernet PHY add-on board to be used with Arm-based, high-performance microcontroller evaluation modules. This add-on board is an excellent choice for initial Ethernet evaluation and prototyping using EVMs. DP83867-EVM-AM is equipped with a TI DP83867IR low latency 10/100/1000-Mbps PHY with RGMII interface and a standard RJ45 Ethernet networking connector. DP83867-EVM-AM is supported on EVMs that have an Ethernet expansion connector such as the AUDIO-AM275-EVM.

Features

The Arm-based Processors EVM Industrial Ethernet PHY Add-on Board has the following features:

- DP83867IR low latency 10/100/1000-Mbps Industrial Ethernet PHY with RGMII interface
- Standard RJ45 Ethernet networking connector
- Shielded DF40GB 48-pin connector for interfacing with Arm-based Processors series evaluation modules



1 Evaluation Module Overview

Preface: Read This First

For the proper mounting instructions, please refer to Installation.

Note

TI does **NOT** recommend mounting Ethernet add-on boards without mounting hardware. TI is not responsible for any damaged caused by using the add-on board without the proper mounting hardware installed.

1.1 If You Need Assistance

If you have any feedback or questions, support for the EVM Industrial Ethernet PHY Add-on Board development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in Section 5.1.

1.1 Introduction

The Arm-based processor EVM Industrial Ethernet PHY Add-on Board was developed to enable additional Ethernet peripheral support on various EVMs and allow for rapid prototyping of the core SoC for Industrial Ethernet applications. This User Guide details the design of the add-on board and how to properly use the interface. The User Guide also details many important aspects of the board including, but not limited to pin header descriptions, test points, and signal routing.

1.2 Kit Contents

The EVM Industrial Ethernet PHY Add-on Board kit contains the following items:

- DP83867-EVM-AM Industrial Ethernet PHY Add-on Board
- Board mounting hardware

Not included:

- EVM

Note

DP83867-EVM-AM can be available as a virtual bundle with select EVMs. Visit the EVM product page (DP83867-EVM-AM) for more information.

1.3 Device Information

The DP83867 is a fully featured Physical Layer transceiver with integrated PMD sub-layers to support 10BASETe, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83867 is designed for easy implementation of 10/100/1000Mbps Ethernet LANs. It interfaces directly to twisted pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII), the IEEE 802.3z Gigabit Media Independent Interface (GMII), or Reduced GMII (RGMII).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low jitter, low latency and provides IEEE 1588 Start of Frame Detection for time sensitive protocols.

The DP83867 offers innovative diagnostic features including dynamic link quality monitoring for fault prediction during normal operation. It can support up to 130m cable length.

For additional information, refer to the *DP83867IR Data Sheet*

2 Hardware

2.1 Component Identification

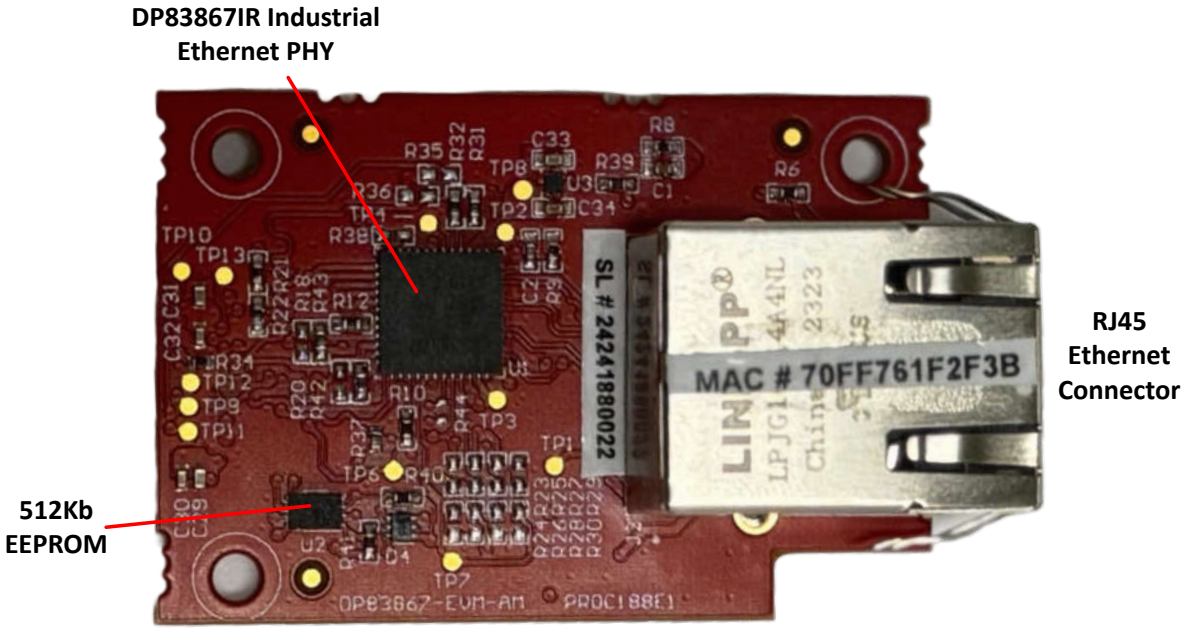


Figure 2-1. DP83867-EVM-AM Top Side

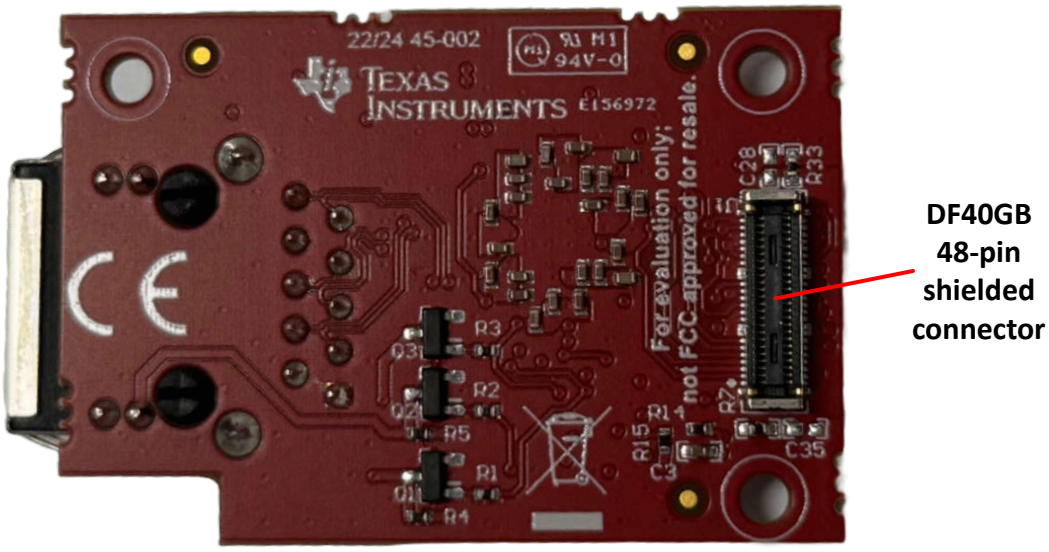


Figure 2-2. DP83867-EVM-AM Bottom Side

2.2 Power Requirements

The EVM Industrial Ethernet PHY Add-on Board is powered from a 3.3V input from the DF40GB 48-pin connector that interfaces the DP83867-EVM-AM with the main EVM. The following sections describe the power distribution network topology that supply the EVM Industrial Ethernet PHY Add-on Board, supporting components, and reference voltages.

2.2.1 Power Tree

The DP83867-EVM-AM power is supplied from the main EVM via the DF40GB connector.

3.3V (VCC_3V3_SYS) is connected to pin 44 and 46 on the DF40GB connector, and is passed to the source input, VDDIO, on the DP83867IR Industrial Ethernet PHY.

2.5V (VDD_2V5) is connected to pin 4 and 6 on the DF40GB connector, and is passed as input to the LDO (TLV75510PDQNR) which outputs 1.0V (VDD_1V0). VDD_2V5 is connected to VDDA_2P5 inputs and VDD_1V0 is connected to VDD1P0 inputs of the Ethernet PHY.

Figure 2-3 shows the power connections of DP83867-EVM-AM.

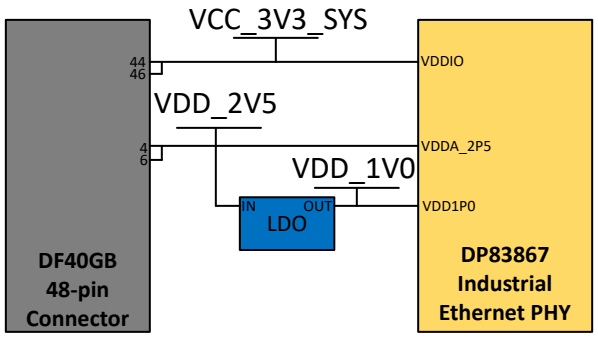


Figure 2-3. Power Tree

2.3 Functional Block Diagram

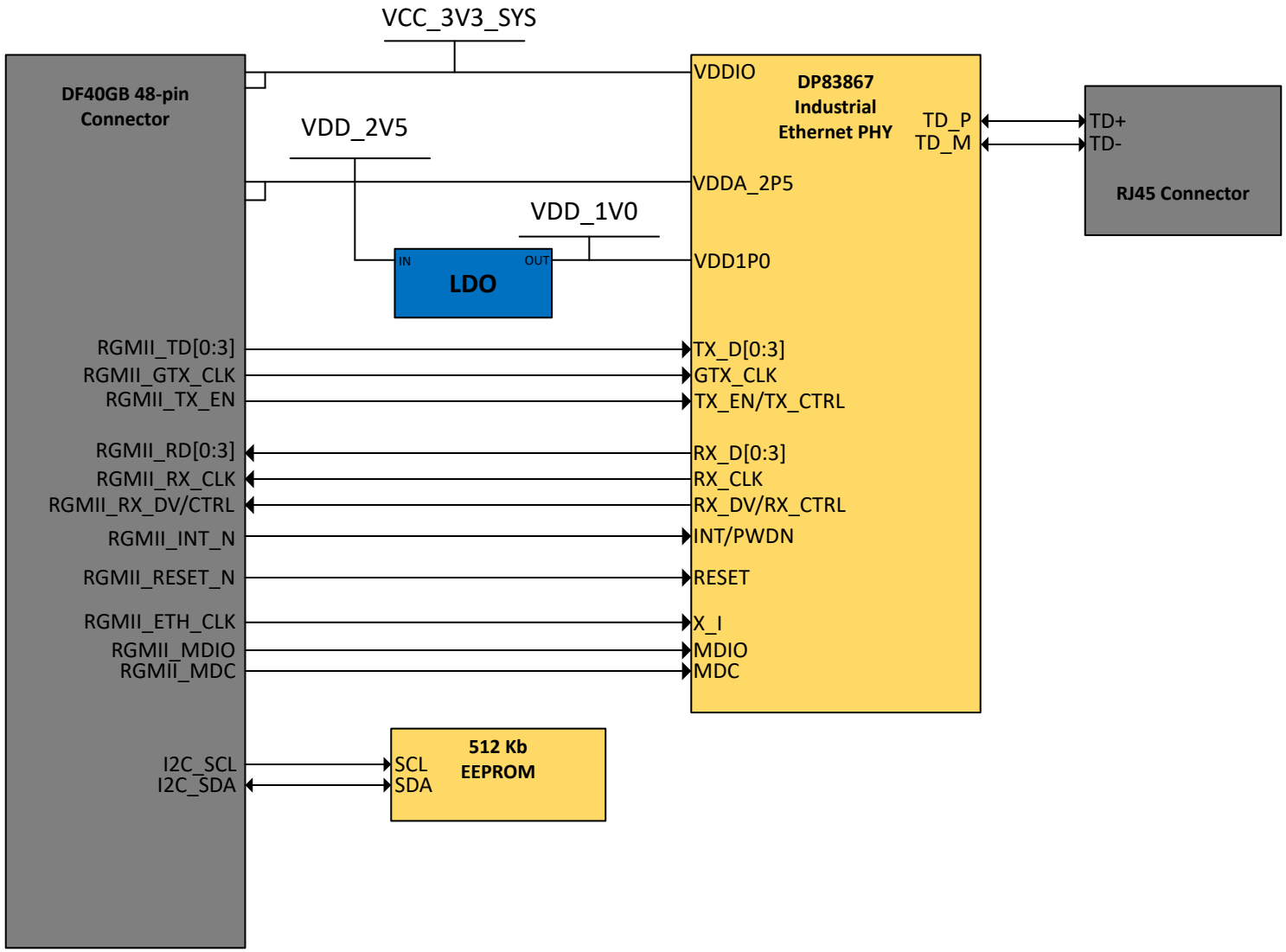


Figure 2-4. AMx Industrial Ethernet PHY Add-on Board Block Diagram

2.4 Header Information

The DP83867-EVM-AM is equipped with a Hirose DF40GB 2x24-pin connector (J1) to connect to AMx EVMs. Listed below are the features of this connector relevant to this EVM:

- 2x24 pins
- Shielded type to support high-speed signals and prevent noise
- High density mounting

Refer to Table 2-1 for a complete list of the header pins and descriptions.

Table 2-1. DF40GB Header Pinout

Pin #	Signal	Description		Description	Signal	Pin #
1	GND	Ground		External Voltage Monitor	EXT_VMON	2
3	TX_CLK	Transmit Clock		2.5V supply	VDD_2V5	4
5	GND	Ground		2.5V supply	VDD_2V5	6
7	TX_D0	Transmit Data 0		Ground	GND	8
9	TX_D1	Transmit Data 1		Interrupt To Ethernet PHY	PWDN/INTn	10
11	TX_D2	Transmit Data 2		Reset input to Ethernet PHY	RESETn	12
13	TX_D3	Transmit Data 3		Collision Detected	COL	14
15	GND	Ground		Ground	GND	16
17	GND	Ground		Ground	GND	18
19	RX_CLK	Receive Clock		MDIO Clock	MDIO_MDC	20
21	GND	Ground		MDIO Data	MDIO_MDIO	22
23	RX_D0	Receive Data 0		Ground	GND	24
25	RX_D1	Receive Data 1		Inhibit	INH	26
27	RX_D2	Receive Data 2		25 MHz Ref. clock	REF_CLK	28
29	RX_D3	Receive Data 3		Carrier Sense	CRS	30
31	GND	Ground		Ground	GND	32
33	GND	Ground		Ground	GND	34
35	TXEN	Transmit Enable		Board Connection Detect	BRD_CONN_DET	36
37	EEPROM_A2	EEPROM I2C Address bit [2]		IEEE 1588 SFD	1588_SFD	38
39	RX_ER	Receive Data Error		I2C Clock	I2C_SCL	40
41	GND	Ground		I2C Data	I2C_SDA	42
43	ETH_GPIO0	ETH GPIO0		IO Voltage Supply	VDDIO	44
45	RXDV	Receive Data Valid		IO Voltage Supply	VDDIO	46
47	EEPROM_A0	EEPROM I2C Address bit [0]		RGMII ETH CLKOUT	CLKOUT	48

2.5 Test Points

DP83867-EVM-AM is equipped with multiple test points for hardware debug and bench testing. Table 2-2 shows the test points on the board and their associated signal net.

Table 2-2. DP83867-EVM-AM Test Points

Test Point	Signal	Description
TP1	VCC	RJ45 VCC
TP2	VDDA1P8	Analog 1.8V Input
TP3	ETH_LED0	Link established indicator
TP4	CLK_OUT	ETH PHY Ref. Clk out
TP5	EXT_VMON	External voltage monitor
TP6	ETH_GPIO0	PHY GPIO0
TP7	ETH_GPIO1	PHY GPIO1
TP8	VDD_1V0	1.0V LDO Output
TP9	INH	Inhibit
TP10	1588_SFD	1588 Start of frame
TP11	COL	Collision detected
TP12	CRS	Carrier sense
TP13	RX_ER	Receive error

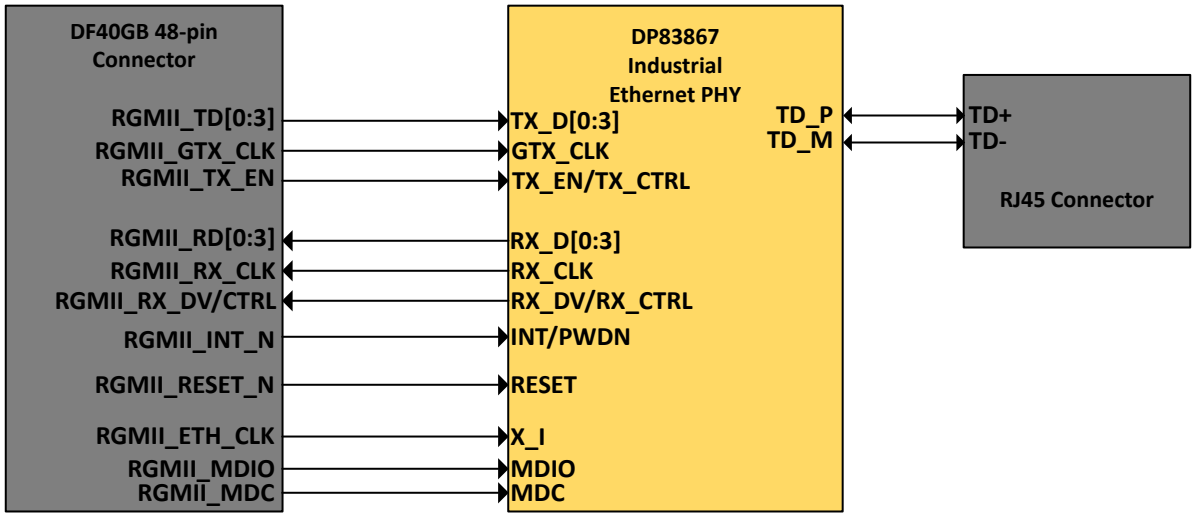
2.6 Interfaces

2.6.1 Ethernet Interface

2.6.1.1 Industrial Ethernet PHY

The AMx EVM Industrial Ethernet PHY Add-on Board uses one port of RGMII signals to be connected to a 32-pin Ethernet PHY (DP83867IR). The PHY is configured to advertise 10/100/1000 Mb operation. The Ethernet data signals of the PHY are terminated to an RJ45 Connector. LEDs are used to indicate link status and activity.

Figure 2-5. Industrial Ethernet PHY



The Ethernet PHY requires three power sources, VDDIO (3.3V or 1.8V), VDDA2P5 (2.5V), and VDD1P0 (VDD_1V0) which are supplied through the DF40GB connector (J1).

On some EVMs, the RGMII port of the CPSW signals are internally muxed on the same balls of the MCU as the PRU-ICSS Ethernet signals. To use RGMII, the balls must be set to the appropriate mux mode for RGMII.

The MDIO and Interrupt signals from the main EVM SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. These resistors are not assembled by default on the DP83867-EVM-AM, but there are footprints if the main EVM does not have these signals pulled up. The interrupt signal is driven by a GPIO signal that is mapped from the main EVM SoC.

The reset signal for the Ethernet PHY is most often driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the main SoC EVM and a reset status signal on the main EVM.

2.6.1.2 Industrial Ethernet PHY Strapping Resistors

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Note

The DP83867-EVM-AM is designed for a VDDIO voltage of 3.3V. If these board is connected to a 1.8V VDDIO system then the strapping resistors will need to be updated. For complete details on the strapping resistor modes, refer to the 4-Level Strap Resistor Ratios table within the *DP83867IR Data Sheet*.

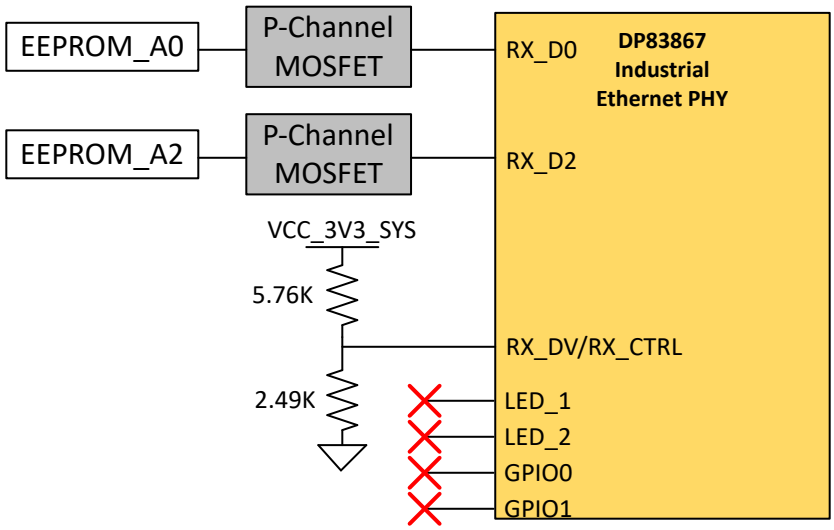


Figure 2-6. Industrial Ethernet PHY Strapping Resistors

Table 2-3. Industrial 10/100/1000 Mbit Ethernet PHY Strapping Resistors

Functional Pin	Mode on DP83867-EVM-AM	Function
RX_D0	EEPROM_A0	PHY address: 0[EEPROM_A2][EEPROM_A0]. See Section 2.6.1.4 for more information on PHY addressing.
RX_D2	EEPROM_A2	
RX_DV/RX_CTRL	3	Auto negotiation enabled
LED_1	1	Clock Skew TX[2] = 2 ns Advertise ability of 10/100/1000 Mbps
LED_2	1	Clock Skew TX[1] = 2 ns Clock Skew TX[0] = 2 ns
GPIO0	1	Clock Skew RX[0] = 2 ns
GPIO1	1	Clock Skew RX[2] = 2 ns Clock Skew RX[1] = 2 ns

2.6.1.3 LED Indication in RJ45 Connector

The EVM Industrial Ethernet PHY Add-on Board has one RJ45 network ports for the RGMII port of the main EVM SoC. The RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

- RJ45 Connector LED indication for the RGMII port:

Table 2-4. ICSSM PRU1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	10BT speed link is up
Left LED	Green	Ethernet activity indicator
	Yellow	GPIO0

2.6.1.4 Multi-Connector Addressing

For AMx EVMs with more than one Ethernet add-on board connector, each DP83867-EVM-AM requires a different EEPROM I2C address and PHY address. The EEPROM A0 and A2 nets, set by pull resistors on the main EVM drive the PHY address nets via a FET network implemented on the DP83867-EVM-AM. Table 2-5 details the multi-connector I2C and PHY addressing scheme implemented on the add-on PHY board.

Note

- The EEPROM I2C address bits A2 and A0 are driven via pull resistors on the main EVM. The pull resistors for each enumerated connector follow the table below.
- EEPROM I2C address bit A1 will **always** be pulled high to VDDIO on the add-on board
- The EEPROM I2C address is defined by the following 8 bits: 8b1010[A2][A1][A0][R/W]
- Pulls to VDDIO/GND are via 10kOhm resistor
- All EVMs with a single connector are configured as CONNECTOR_0

Table 2-5. Multi-Connector I2C / PHY Addressing Scheme

Connector_#	EEPROM_A2 (connector pin 37)		EEPROM_A1		EEPROM_A0 (connector pin 47)		I2C Address	DP83867 PHY Address
	Pull	A2	Pull	A1	Pull	A0		
CONNECTOR_0	GND	0	VDDIO	1	GND	0	0x52	5b00000
CONNECTOR_1	GND	0	VDDIO	1	VDDIO	1	0x53	5b00001
CONNECTOR_2	VDDIO	1	VDDIO	1	GND	0	0x56	5b00100
CONNECTOR_3	VDDIO	1	VDDIO	1	VDDIO	1	0x57	5b00101

2.7 Integration Guide

The AMx Ethernet Add-on Board ecosystem is not limited to the DP83867 Industrial Ethernet PHY. A wide variety of Industrial Ethernet PHYs with Arm-based processor compatible signals can be designed onto add-on boards to be used across different compatible EVMs. This section details the mechanical information and provide the necessary dimensions for designing an Industrial Ethernet PHY add-on board.

Note

All dimensions are measured in inches.

2.7.1 Board Dimensions

Figure 2-7 shows the proper PCB dimensions for an Industrial Ethernet PHY add-on board to be compatible with AMx EVMs.

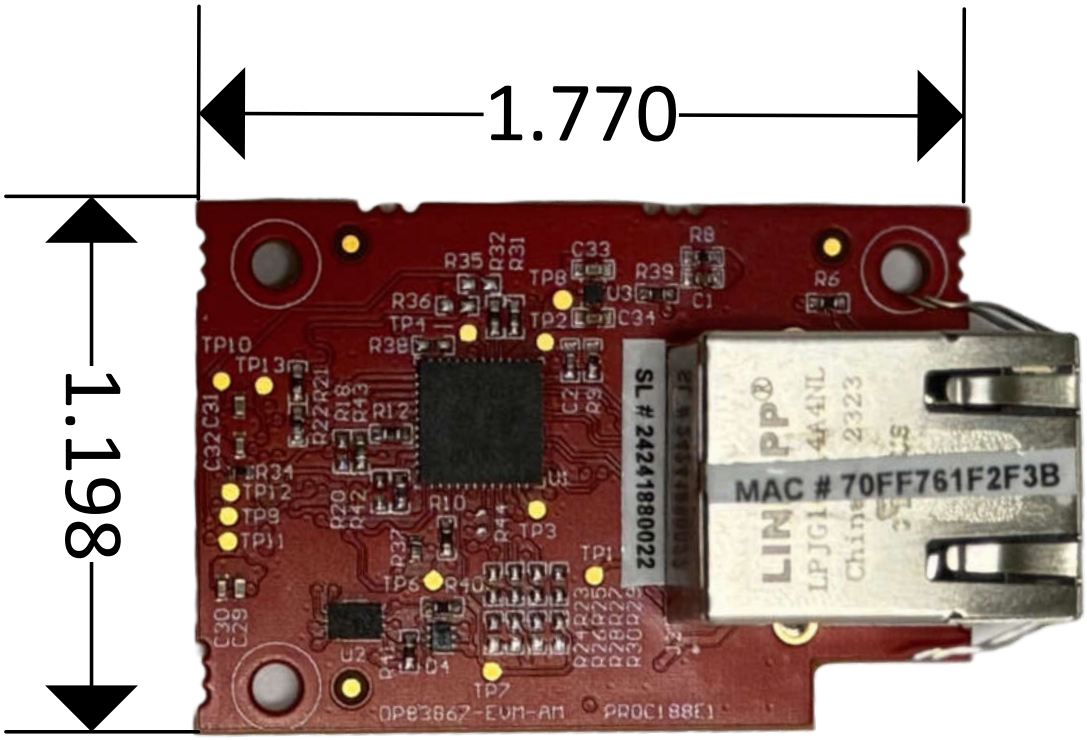


Figure 2-7. Industrial Ethernet PHY Add-on Board Dimensions

2.7.2 Installation

The Add-on board kit includes mounting hardware to install the board onto any compatible Arm-based processors EVMs.

The mounting hardware includes the following:

- 3x M3 Screws
- 3x plastic washers
- 3x metal nuts
- 3x plastic spacers

Below is the recommended method of mounting the add-on board:

1. Place the plastic washers on all screws
2. Place the screw with washers in the mounting holes of the add-on board
3. On the main EVM, place the plastic spacers on top of the main EVM mounting holes for the corresponding connector
4. Align the screws of the add-on board with the plastic spacers and main EVM mounting holes
5. Press down on the add-on board until there is an audible click signifying the connectors are flush
6. Thread the metal nuts on the underside of the main EVM on the screws until there is a secure connection between the add-on board and main EVM

Note

TI does **NOT** recommend mounting any Ethernet Add-on cards to the EVM without the mounting hardware. Doing so may cause damage to either or both boards.

3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, go to the EVM product page on ti.com (DP83867-EVM-AM).

4 Additional Information

4.1 Trademarks

E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM275x Audio Evaluation Module Tool Folder*
- *AM62Dx Audio Evaluation Module Tool Folder*
- *DP83867IR Datasheet*
- *DP83867IR Product Folder*
- *Texas Instruments Code Composer Studio*

6 Revision History

DATE	REVISION	NOTES
January 2025	*	Initial Release

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