TMS320x2834x Delfino High Resolution Pulse Width Modulator (HRPWM)

Reference Guide

Literature Number: SPRUG77B
September 2009–Revised October 2011

Contents

List of Figures

List of Tables

Read This First

About This Manual

This document describes the operation of the high-resolution extension to the pulse width modulator (HRPWM) on the TMS320x2834x Delfino™ device . The HRPWM module described in this reference guide is a Type 0 HRPWM. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566) for a list of all devices with an HRPWM module of the same type, to determine the differences between types, and for a list of device-specific differences within a type.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C2000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the 2834x Delfino™ devices, related peripherals, and other technical collateral, is available in the C2000 DSP product folder at: www.ti.com/c2000.

Data Manual—

SPRS516 — TMS320C28346, TMS320C28345, TMS320C28344, TMS320C28343, TMS320C28342, TMS320C28341 Delfino Microcontrollers Data Manual. This document contains the pinout, signal descriptions, as well as electrical and timing specifications for the C2834x devices.

SPRZ267 — TMS320C2834x Delfino MCU Silicon Errata. This document describes the advisories and usage notes for different versions of silicon.

CPU User's Guides—

SPRU430 — TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

SPRUEO2 — TMS320C28x Floating Point Unit and Instruction Set Reference Guide. This document describes the floating-point unit and includes the instructions for the FPU.

Peripheral Guides—

SPRU566 — TMS320x28xx, 28xxx DSP Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUFN1 — TMS320x2834x Delfino System Control and Interrupts Reference Guide. This document describes the various interrupts and system control features of the x2834x microcontroller (MCUs).

SPRUFN4 — **TMS320x2834x Delfino External Interface (XINTF) Reference Guide**. This document describes the XINTF, which is a nonmultiplexed asynchronous bus, as it is used on the x2834x device.

SPRUFN5 — **TMS320x2834x Delfino Boot ROM Reference Guide**. This document describes the purpose and features of the bootloader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUG80 — **TMS320x2834x Delfino Multichannel Buffered Serial Port (McBSP) Reference Guide**. This document describes the McBSP available on the x2834x devices. The McBSPs allow direct interface between a microcontroller (MCU) and other devices in a system.

SPRUG78 — **TMS320x2834x Delfino Direct Memory Access (DMA) Reference Guide**. This document describes the DMA on the x2834x microcontroller (MCUs).

SPRUFZ6 — **TMS320x2834x Delfino Enhanced Pulse Width Modulator (ePWM) Module Reference Guide**. This document describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRUG77 — **TMS320x2834x Delfino High-Resolution Pulse Width Modulator (HRPWM) Reference Guide**. This document describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRUG79 — **TMS320x2834x Delfino Enhanced Capture (eCAP) Module Reference Guide**. This document describes the enhanced capture module. It includes the module description and registers.

SPRUG74 — **TMS320x2834x Delfino Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide**. This document describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

SPRUEU4 — **TMS320x2834x Delfino Enhanced Controller Area Network (eCAN) Reference Guide**. This document describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments.

SPRUG75 — **TMS320x2834x Delfino Serial Communication Interface (SCI) Reference Guide**. This document describes the SCI, which is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

SPRUG73 — **TMS320x2834x Delfino Serial Peripheral Interface (SPI) Reference Guide**. This document describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRUG76 — **TMS320x2834x Delfino Inter-Integrated Circuit (I2C) Reference Guide**. This document describes the features and operation of the inter-integrated circuit (I2C) module.

Tools Guides—

SPRU513 — **TMS320C28x Assembly Language Tools v5.0.0 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 — **TMS320C28x Optimizing C/C++ Compiler v5.0.0 User's Guide** describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 — **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

SPRU625 — **TMS320C28x DSP/BIOS 5.32 Application Programming Interface (API) Reference Guide** describes development using DSP/BIOS.

Application Reports—

SPRAB26 — **TMS320x2833x/2823x to TMS320x2834x Delfino Migration Overview**. This application report describes differences between the Texas Instruments TMS320x2833x/2823x and the TMS320x2834x devices to assist in application migration.

High-Resolution Pulse Width Modulator (HRPWM)

This document is used in conjunction with the device-specific *Enhanced Pulse Width Modulator (ePWM) Module Reference Guide.*

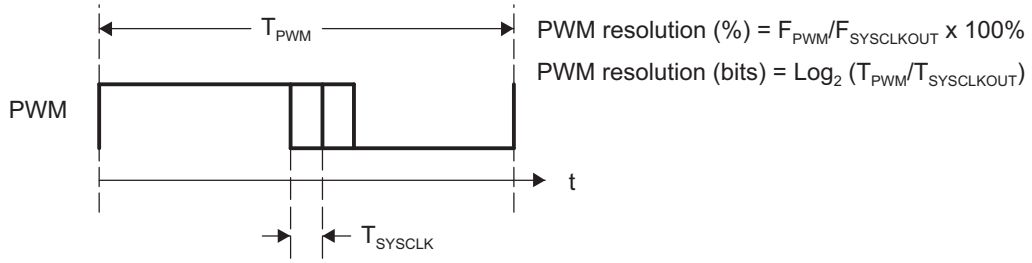
The HRPWM module extends the time resolution capabilities of the conventionally derived digital pulse width modulator (PWM). HRPWM is typically used when PWM resolution falls below ~ 9-10 bits. The key features of HRPWM are:

- Extended time resolution capability
- Used in both duty cycle and phase-shift control methods
- Finer time granularity control or edge positioning using extensions to the Compare A and Phase registers
- Implemented using the A signal path of PWM, i.e., on the EPWMxA output.
- Self-check diagnostics software mode to check if the micro edge positioner (MEP) logic is running optimally

1 Introduction

The ePWM peripheral is used to perform a function that is mathematically equivalent to a digital-to-analog converter (DAC). As shown in Figure 1, the effective resolution for conventionally generated PWM is a function of PWM frequency (or period) and system clock frequency.

Figure 1. Resolution Calculations for Conventionally Generated PWM



If the required PWM operating frequency does not offer sufficient resolution in PWM mode, you may want to consider HRPWM. As an example of improved performance offered by HRPWM, Table 1 shows resolution in bits for various PWM frequencies. These values assume a MEP step size of 60 ps. See the device-specific datasheet for typical and maximum performance specifications for the MEP.

Table 1. Resolution for PWM and HRPWM

PWM Freq	Regular Resolution (PWM)				High Resolution (HRPWM)	
	300 MHz SYSCLKOUT		200 MHz SYSCLKOUT			
(kHz)	Bits	%	Bits	%	Bits	%
20	13.9	0.0	13.3	0.0	0.0	0.000
50	12.6	0.0	12.0	0.0	18.3	0.000
100	11.6	0.0	11.0	0.1	17.3	0.001
150	11.0	0.1	10.4	0.1	16.8	0.001
200	10.6	0.1	10.0	0.1	16.3	0.001

Table 1. Resolution for PWM and HRPWM (continued)

250	10.2	0.1	9.6	0.1	16.0	0.002
500	9.2	0.2	8.6	0.3	15.0	0.003
1000	8.2	0.3	7.6	0.5	14.0	0.006
1500	7.6	0.5	7.1	0.8	13.4	0.009
2000	7.2	0.7	6.6	1.0	13.0	0.012

Although each application may differ, typical low frequency PWM operation (below 250 kHz) may not require HRPWM. HRPWM capability is most useful for high frequency PWM requirements of power conversion topologies such as:

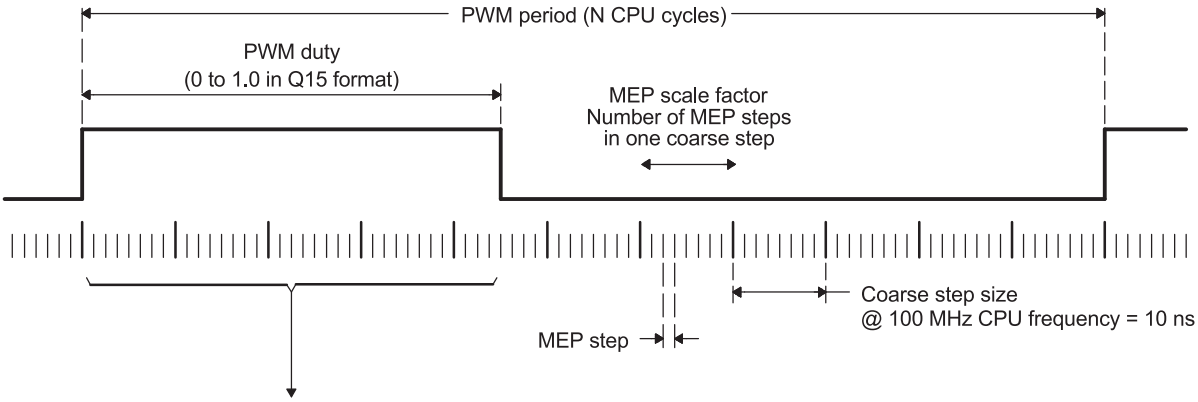
- Single-phase buck, boost, and flyback
- Multi-phase buck, boost, and flyback
- Phase-shifted full bridge
- Direct modulation of D-Class power amplifiers

2 Operational Description of HRPWM

The HRPWM is based on micro edge positioner (MEP) technology. MEP logic is capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. The time step accuracy is on the order of 60 ps. See the device-specific data sheet for the typical MEP step size on a particular device. The HRPWM also has a self-check software diagnostics mode to check if the MEP logic is running optimally, under all operating conditions. Details on software diagnostics and functions are in Section 2.4.

Figure 2 shows the relationship between one coarse system clock and edge position in terms of MEP steps, which are controlled via an 8-bit field in the Compare A extension register (CMPAHR).

Figure 2. Operating Logic Using MEP



Number of coarse steps = integer(PWMduty * PWMperiod)
Number of MEP steps = fraction(PWMduty * PWMperiod) * (MEPScaleFactor)

16−bit CMPA register value	= number of coarse steps
16−bit CMPAHR register value	[(number of MEP steps) +1.5†]<< 8

† For MEP range and rounding adjustment (0x0180 in Q8 format)

To generate an HRPWM waveform, configure the TBM, CCM, and AQM registers as you would to generate a conventional PWM of a given frequency and polarity. The HRPWM works together with the TBM, CCM, and AQM registers to extend edge resolution, and should be configured accordingly. Although many programming combinations are possible, only a few are needed and practical. These methods are described in Section 2.5.

Registers discussed but not found in this document can be seen in the device-specific *Enhanced Pulse Width Modulator (ePWM) Module Reference Guide*.

The HRPWM operation is controlled and monitored using the following registers:

Table 2. HRPWM Registers

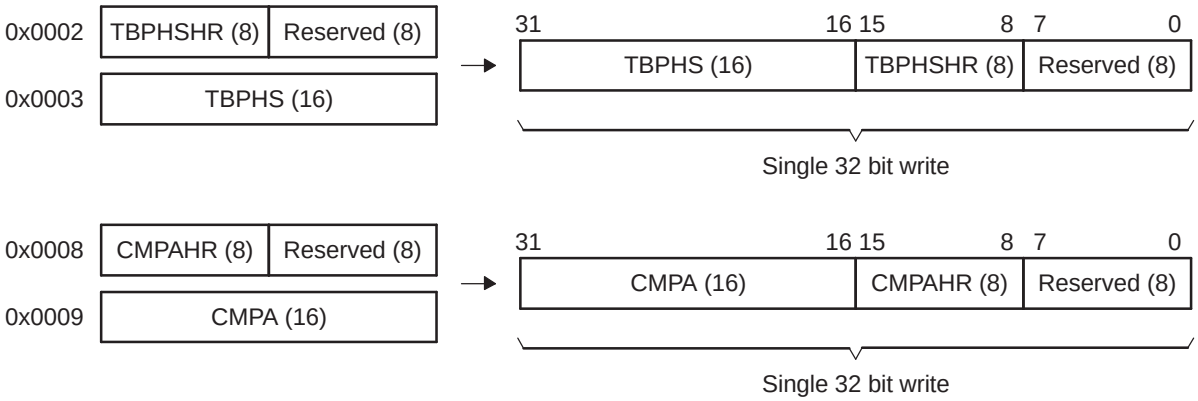
mnemonic	Address Offset	Shadowed	Description
TBPHSHR	0x0002	No	Extension Register for HRPWM Phase (8 bits)
CMPAHR	0x0008	Yes	Extension Register for HRPWM Duty (8 bits)
HRCNFG	0x0020	No	HRPWM Configuration Register

2.1 Controlling the HRPWM Capabilities

The MEP of the HRPWM is controlled by two extension registers, each 8-bits wide. These two HRPWM registers are concatenated with the 16-bit TBPHS and CMPA registers used to control PWM operation.

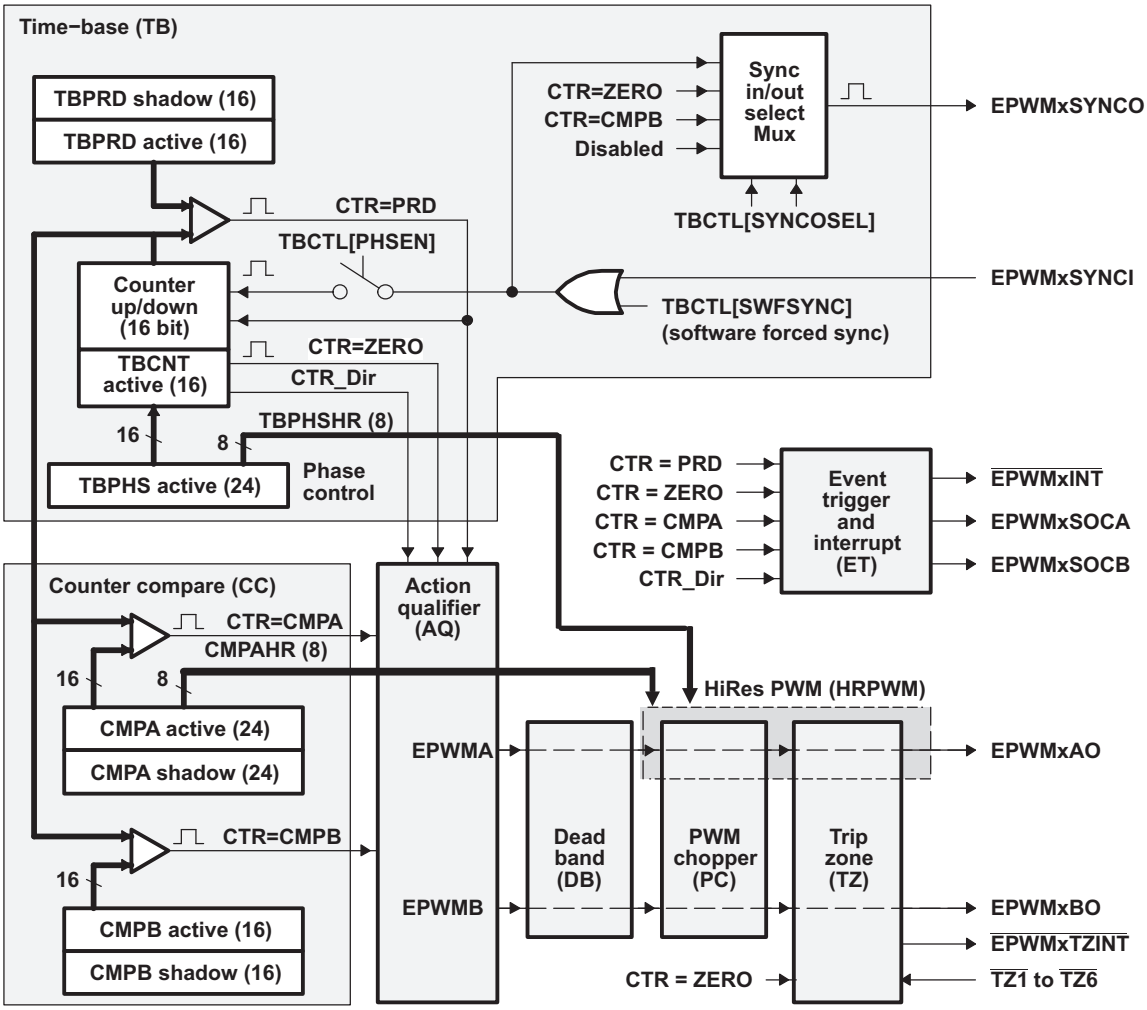
- TBPHSHR - Time Base Phase High Resolution Register
- CMPAHR - Counter Compare A High Resolution Register

Figure 3. HRPWM Extension Registers and Memory Configuration



HRPWM capabilities are controlled using the Channel A PWM signal path. Figure 4 shows how the HRPWM interfaces with the 8-bit extension registers.

Figure 4. HRPWM System Interface



2.2 Configuring the HRPWM

Once the ePWM has been configured to provide conventional PWM of a given frequency and polarity, the HRPWM is configured by programming the HRCNFG register located at offset address 20h. This register provides configuration options for the following key operating modes:

Edge Mode — The MEP can be programmed to provide precise position control on the rising edge (RE), falling edge (FE) or both edges (BE) at the same time. FE and RE are used for power topologies requiring duty cycle control, while BE is used for topologies requiring phase shifting, e.g., phase shifted full bridge.

Control Mode — The MEP is programmed to be controlled either from the CMPAHR register (duty cycle control) or the TBPHSHR register (phase control). RE or FE control mode should be used with CMPAHR register. BE control mode should be used with TBPHSHR register.

Shadow Mode — This mode provides the same shadowing (double buffering) option as in regular PWM mode. This option is valid only when operating from the CMPAHR register and should be chosen to be the same as the regular load option for the CMPA register. If TBPHSHR is used, then this option has no effect.

2.3 Principle of Operation

The MEP logic is capable of placing an edge in one of 255 (8 bits) discrete time steps (see device-specific data sheet for typical MEP step size). The MEP works with the TBM and CCM registers to be certain that time steps are optimally applied and that edge placement accuracy is maintained over a wide range of PWM frequencies, system clock frequencies and other operating conditions. Table 3 shows the typical range of operating frequencies supported by the HRPWM.

Table 3. Relationship Between MEP Steps, PWM Frequency and Resolution

System (MHz)	MEP Steps Per SYSCLKOUT (1) (2) (3)	PWM MIN (Hz) (4)	PWM MAX (MHz)	Res. @ MAX (Bits) (5)
200	83	3052	10	10.7
225	74	3433	11.25	10.5
250	67	3815	12.5	10.4
275	61	4196	13.75	10.2
300	56	4578	15	10.1

(1) System frequency = SYSCLKOUT, i.e., CPU clock. TBCLK =SYSCLKOUT.
(2) Table data based on a MEP time resolution of 60 ps (this is an example value, see the device-specific data sheet for MEP limits.
(3) MEP steps applied = $T_{SYSCLKOUT}$/60 ps in this example.
(4) PWM minimum frequency is based on a maximum period value, i.e., TBPRD = 65535. PWM mode is asymmetrical up-count.
(5) Resolution in bits is given for the maximum PWM frequency stated.

2.3.1 Edge Positioning

In a typical power control loop (e.g., switch modes, digital motor control [DMC], uninterruptible power supply [UPS]), a digital controller (PID, 2pole/2zero, lag/lead, etc.) issues a duty command, usually expressed in a per unit or percentage terms. Assume that for a particular operating point, the demanded duty cycle is 0.405 or 40.5% on time and the required converter PWM frequency is 1.25 MHz. In conventional PWM generation with a system clock of 300 MHz, the duty cycle choices are in the vicinity of 40.5%. In Figure 5, a compare value of 97 counts (i.e., duty = 40.42%) is the closest to 40.5% that you can attain. This is equivalent to an edge position of 323 ns instead of the desired 324 ns. This data is shown in Table 4.

By utilizing the MEP, you can achieve an edge position much closer to the desired point of 324 ns. Table 4 shows that in addition to the CMPA value, 11 steps of the MEP (CMPAHR register) will position the edge at 323.9 9 ns, resulting in almost zero error. In this example, it is assumed that the MEP has a step resolution of 60 ps.

Figure 5. Required PWM Waveform for a Requested Duty = 40.5%

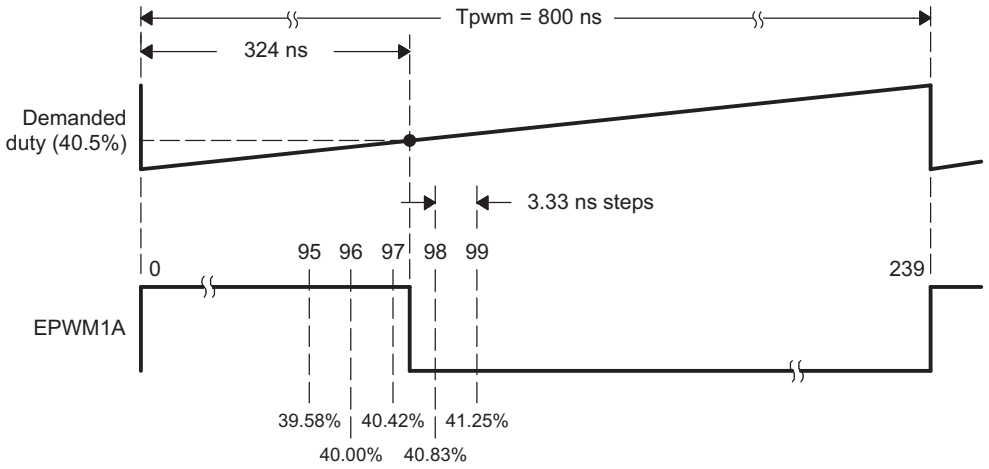


Table 4. CMPA vs Duty (left), and [CMPA:CMPAHR] vs Duty (right)

CMPA (count) (1) (2) (3)	Duty %	High Time (ns)	CMPA (count)	CMPAHR (count)	Duty (%)	High Time (ns)
93	38.75%	310	97	4	40.45%	323.57
94	39.17%	313	97	5	40.45%	323.63
95	39.58%	317	97	6	40.46%	323.69
96	40.00%	320	97	7	40.47%	323.75
97	40.42%	323	97	8	40.48%	323.81
98	40.83%	327	97	9	40.48%	323.87
99	41.25%	330	97	10	40.49%	323.93
			97	11	40.50%	323.99
Required			97	12	40.51%	324.05
97.2	40.50%	324	97	13	40.51%	324.11

(1) System clock, SYSCLKOUT and TBCLK = 300 MHz, 3.33 ns
(2) For a PWM Period register value of 240 counts, PWM Period = 240 x 3.33 ns = 800 ns, PWM frequency = 1/800 ns = 1.25 MHz
(3) Assumed MEP step size for the above example = 60 ps
See the device-specific data manual for typical and maximum MEP values.

2.3.2 Scaling Considerations

The mechanics of how to position an edge precisely in time has been demonstrated using the resources of the standard CMPA and MEP (CMPAHR) registers. In a practical application, however, it is necessary to seamlessly provide the CPU a mapping function from a per-unit (fractional) duty cycle to a final integer (non-fractional) representation that is written to the [CMPA:CMPAHR] register combination.

To do this, first examine the scaling or mapping steps involved. It is common in control software to express duty cycle in a per-unit or percentage basis. This has the advantage of performing all needed math calculations without concern for the final absolute duty cycle, expressed in clock counts or high time in ns. Furthermore, it makes the code more transportable across multiple converter types running different PWM frequencies.

To implement the mapping scheme, a two-step scaling procedure is required.

Assumptions for this example:

System clock , SYSCLKOUT	=	3.33 ns (300 MHz)
PWM frequency	=	1.25 MHz (1/800 ns)
Required PWM duty cycle, **PWMDuty**	=	0.405 (40.5%)
PWM period in terms of coarse steps, **PWMperiod** (800 ns/ 3.33 ns)	=	240
Number of MEP steps per coarse step at 60 ps (3.33 ns / 60 ps), **MEP_ScaleFactor**	=	55
Value to keep CMPAHR within the range of 1-255 and fractional rounding constant (default value)	=	1.5 (0180h in Q8 format)

Step 1: Percentage Integer Duty value conversion for CMPA register

CMPA register value	=	int(**PWMDuty*****PWMperiod**); int means integer part
	=	int(0.405* 240)
	=	int(97.2)
CMPA register value	=	97 (61h)

Step 2: Fractional value conversion for CMPAHR register

CMPAHR register value	=	(frac(**PWMDuty*****PWMperiod**)***MEP_ScaleFactor** << 8) + 01 80h; frac means fractional part
	=	(frac(97.2)*55 <<8) + 01 80h; Shift is to move the value as CMPAHR high byte
	=	((0.2*55) <<8) + 0 1 80h
	=	(11 <<8) + 0 180h
	=	11*256 + 0 1 80h; Shifting left by 8 is the same as multiplying by 256.
	=	2816 + 0 1 80h
		B 00h + 0 1 80h
CMPAHR value	=	C 80h; CMPAHR value = 0C 00h, lower 8 bits will be ignored by hardware.

NOTE: The MEP scale factor (MEP_ScaleFactor) varies with the system clock and DSP operating conditions. TI provides an MEP scale factor optimizing (SFO) software C function, which uses the built in diagnostics in each HRPWM and returns the best scale factor for a given operating point.

The scale factor varies slowly over a limited range so the optimizing C function can be run very slowly in a background loop.

The CMPA and CMPAHR registers are configured in memory so that the 32-bit data capability of the 28x CPU can write this as a single concatenated value, i.e., [CMPA:CMPAHR].

The mapping scheme has been implemented in both C and assembly, as shown in Section 2.5. The actual implementation takes advantage of the 32-bit CPU architecture of the 28xx, and is somewhat different from the steps shown in Section 2.3.2.

For time critical control loops where every cycle counts, the assembly version is recommended. This is a cycle optimized function (11 SYSCLKOUT cycles) that takes a Q15 duty value as input and writes a single [CMPA:CMPAHR] value.

2.3.3 Duty Cycle Range Limitation

In high resolution mode, the MEP is not active for 100% of the PWM period. It becomes operational:

- 3 SYSCLK cycles after the period starts when diagnostics are disabled
- 6 SYSCLK cycles after the period starts when SFO diagnostics are running

Duty cycle range limitations are illustrated in Figure 6. This limitation imposes a lower duty cycle limit on the MEP. For example, precision edge control is not available all the way down to 0% duty cycle. Although for the first 3 or 6 cycles, the HRPWM capabilities are not available, regular PWM duty control is still fully operational down to 0% duty. In most applications this should not be an issue as the controller regulation point is usually not designed to be close to 0% duty cycle. To better understand the useable duty cycle range, see Table 5 .

Figure 6. Low % Duty Cycle Range Limitation Example When PWM Frequency = 1 MHz

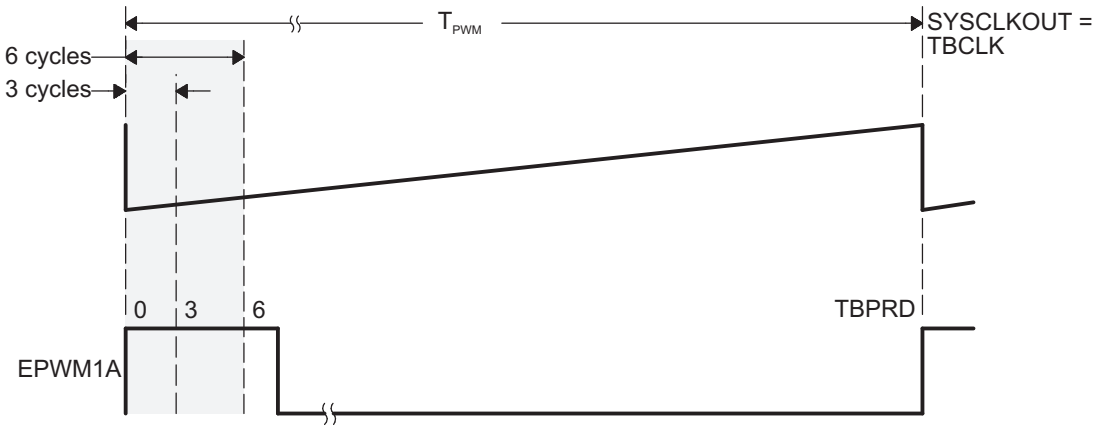


Table 5. Duty Cycle Range Limitation for 3 and 6 SYSCLK/TBCLK Cycles

PWM Frequency (kHz) (1)	3 Cycles Minimum Duty	6 Cycles Minimum Duty
200	0.20%	0.40%
400	0.40%	0.80%
600	0.60%	1.20%

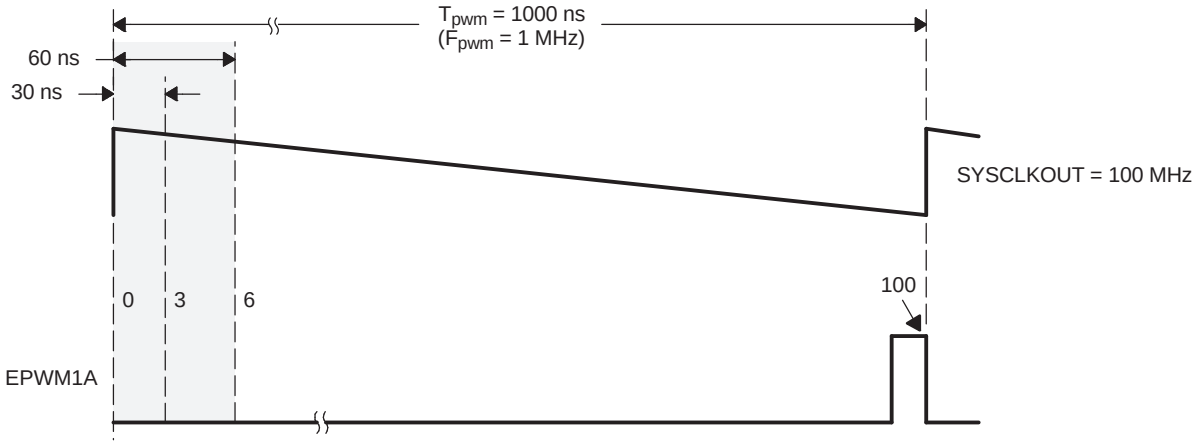
(1) System clock - T = 3.33 ns
System clock = TBCLK = 300 MHz

Table 5. Duty Cycle Range Limitation for 3 and 6 SYSCLK/TBCLK Cycles (continued)

PWM Frequency (kHz) [1]	3 Cycles Minimum Duty	6 Cycles Minimum Duty
800	0.80%	1.60%
1000	1.00%	2.00%
1200	1.20%	2.40%
1400	1.40%	2.80%
1600	1.60%	3.20%
1800	1.80%	3.60%
2000	2.00%	4.00%

If the application demands HRPWM operation in the low percent duty cycle region, then the HRPWM can be configured to operate in count-down mode with the rising edge position (REP) controlled by the MEP. This is illustrated in Figure 7. In this case, low percent duty limitation is no longer an issue. However, there will be a maximum duty limitation with same percent numbers as given in .

Figure 7. High % Duty Cycle Range Limitation Example



2.4 Scale Factor Optimizing Software (SFO)

The micro edge positioner (MEP) logic is capable of placing an edge in one of 255 discrete time steps. As previously mentioned, the size of these steps is on the order of 60 ps (see device-specific data sheet for typical MEP step size on your device). The MEP step size varies based on worst-case process parameters, operating temperature, and voltage. MEP step size increases with decreasing voltage and increasing temperature and decreases with increasing voltage and decreasing temperature. Applications that use the HRPWM feature should use the TI-supplied MEP scale factor optimizer (SFO) software function. The SFO function helps to dynamically determine the number of MEP steps per SYSCLKOUT period while the HRPWM is in operation.

To utilize the MEP capabilities effectively during the Q15 duty to [CMPA:CMPAHR] mapping function (see Section 2.3.2), the correct value for the MEP scaling factor (MEP_ScaleFactor) needs to be known by the software. To accomplish this, each HRPWM module has built in self-check and diagnostics capabilities that can be used to determine the optimum MEP_ScaleFactor value for any operating condition. TI provides a C-callable library containing two SFO function s that utilize this hardware and determines the optimum MEP_ScaleFactor. As such, MEP Control and Diagnostics registers are reserved for TI use.

2.5 HRPWM Examples Using Optimized Assembly Code

The best way to understand how to use the HRPWM capabilities is through two real examples:

1. Simple buck converter using asymmetrical PWM (i.e. count-up) with active high polarity.
2. DAC function using simple R+C reconstruction filter.

The following examples all have Initialization/configuration code written in C. To make these easier to understand, the #defines shown below are used. Note, #defines introduced in *TMS320x2834x Delfino™ Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRU791) are also used.

Example 1 This example assumes MEP step size of 60 ps and does not use the SFO library.

Example 1. #Defines for HRPWM Header Files

```
//---------------------------------
// HRPWM (High Resolution PWM)
//=================================
// HRCNFG
#define HR_Disable 0x0
#define HR_REP 0x1        // Rising Edge position
#define HR_FEP 0x2        // Falling Edge position
#define HR_BEP 0x3        // Both Edge position
#define HR_CMP 0x0        // CMPAHR controlled
#define HR_PHS 0x1        // TBPHSHR controlled
#define HR_CTR_ZERO 0x0   // CTR = Zero event
#define HR_CTR_PRD 0x1    // CTR = Period event
```

2.5.1 Implementing a Simple Buck Converter

In this example, the PWM requirements are:

- PWM frequency = 1 MHz (i.e., TBPRD = 300)
- PWM mode = asymmetrical, up-count
- Resolution = 14 bits (with a MEP step size of 60 ps)

Figure 8 and Figure 9 show the required PWM waveform. As explained previously, configuration for the ePWM1 module is almost identical to the normal case except that the appropriate MEP options need to be enabled/selected.

Figure 8. Simple Buck Controlled Converter Using a Single PWM

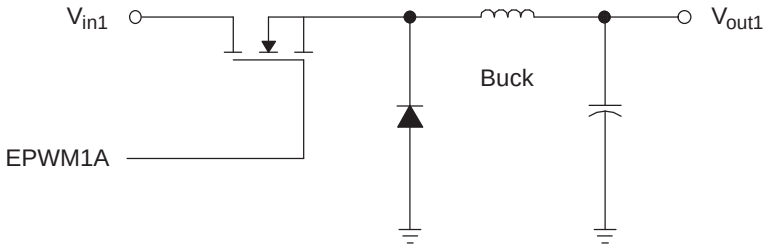
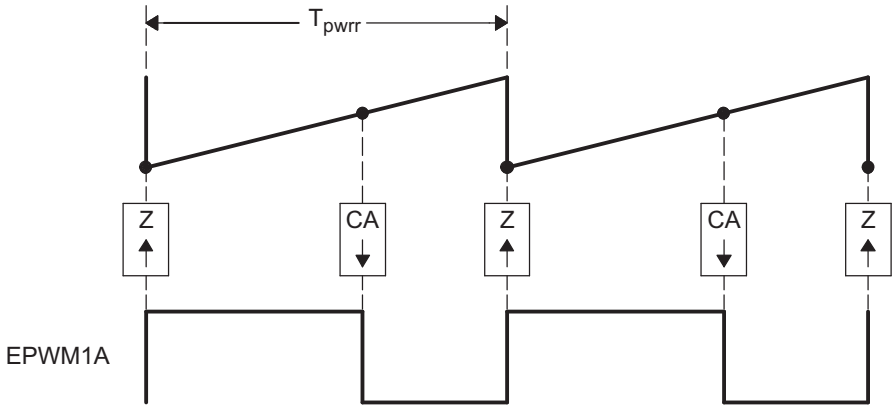


Figure 9. PWM Waveform Generated for Simple Buck Controlled Converter



The example code shown consists of two main parts:

- Initialization code (executed once)
- Run time code (typically executed within an ISR)

Example 2 shows the Initialization code. The first part is configured for conventional PWM. The second part sets up the HRPWM resources.

This example assumes MEP step size of 60 ps and does not use the SFO library.

Example 2. HRPWM Buck Converter Initialization Code

```
void HrBuckDrvCnf(void)
{
    // Config for conventional PWM first
       EPwm1Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;         // set Immediate load
       EPwm1Regs.TBPRD = 300;                            // Period set for 1000 kHz PWM
       hrbuck_period = 600;                              // Used for Q15 to Q0 scaling
       EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
       EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;           // EPWM1 is the Master
       EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
       EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
       EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
    // Note: ChB is initialized here only for comparison purposes, it is not required

       EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
       EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
       EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;     // optional
       EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;       // optional

       EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
       EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
       EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;                // optional
       EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;              // optional
    // Now configure the HRPWM resources
       EALLOW;                                           // Note these registers are protected
                                                         // and act only on ChA
EPwm1Regs.HRCNFG.all = 0x0;                              // clear all bits first
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP;                   // Control Falling Edge Position
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;                   // CMPAHR controls the MEP
EPwm1Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;               // Shadow load on CTR=Zero
EDIS;
MEP_ScaleFactor = 55*256;                               // Start with typical Scale Factor
                                                        // value for 300 MHz
                                                        // Note: Use SFO functions to update


                                                        // MEP_ScaleFactor dynamically
}
```

Example 3 shows an assembly example of run-time code for the HRPWM buck converter.

Example 3. HRPWM Buck Converter Run-Time Code

```
EPWM1_BASE .set 0x6800
CMPAHR1 .set EPWM1_BASE+0x8
;================================================
HRBUCK_DRV; (can execute within an ISR or loop)
;================================================
    MOVW DP, #_HRBUCK_In
    MOVL XAR2,@_HRBUCK_In      ; Pointer to Input Q15 Duty (XAR2)
    MOVL XAR3,#CMPAHR1         ; Pointer to HRPWM CMPA reg (XAR3)
; Output for EPWM1A (HRPWM)
    MOV T,*XAR2                ; T <= Duty
```

Example 3. HRPWM Buck Converter Run-Time Code (continued)

```
    MPYU ACC,T,@_hrbuck_period ; Q15 to Q0 scaling based on Period
    MOV T,@_MEP_ScaleFactor             ; MEP scale factor (from optimizer s/w)
    MPYU P,T,@AL               ; P <= T * AL, Optimizer scaling
    MOVH @AL,P                 ; AL <= P, move result back to ACC
    ADD ACC, #0x180            ; MEP range and rounding adjustment
    MOVL *XAR3,ACC             ; CMPA:CMPAHR(31:8) <= ACC
; Output for EPWM1B (Regular Res) Optional - for comparison purpose only
    MOV *+XAR3[2],AH           ; Store ACCH to regular CMPB
```

2.5.2 Implementing a DAC function Using an R+C Reconstruction Filter

In this example, the PWM requirements are:

- PWM frequency = 400 kHz (i.e., TBPRD = 750)
- PWM mode = Asymmetrical, Up-count
- Resolution = 15.3 bits (MEP step size = 150 ps)

Figure 10 and Figure 11 show the DAC function and the required PWM waveform. As explained previously, configuration for the ePWM1 module is almost identical to the normal case except that the appropriate MEP options need to be enabled/selected.

Figure 10. Simple Reconstruction Filter for a PWM Based DAC

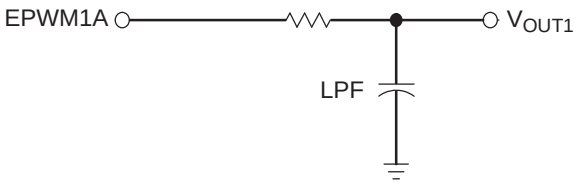
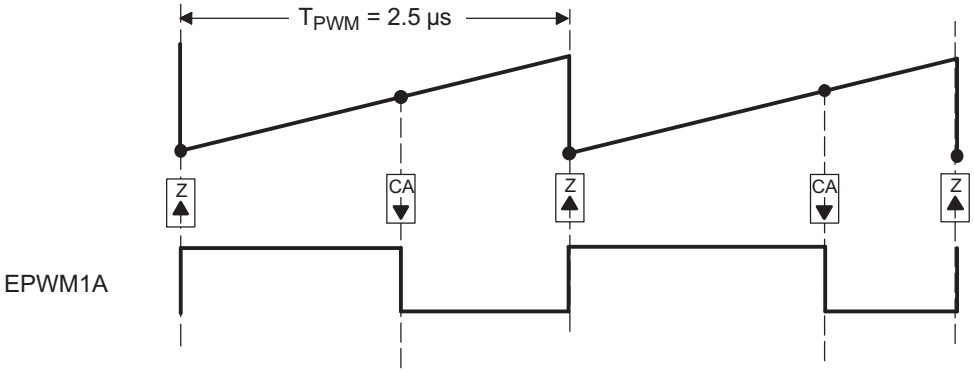


Figure 11. PWM Waveform Generated for the PWM DAC Function



The example code shown consists of two main parts:

- Initialization code (executed once)
- Run time code (typically executed within an ISR)

This example assumes a typical MEP_ScaleFactor and does not use the SFO library.

Example 4 shows the Initialization code. The first part is configured for conventional PWM. The second part sets up the HRPWM resources.

Example 4. PWM DAC Function Initialization Code

```
void HrPwmDacDrvCnf(void)
{
          // Config for conventional PWM first

             EPwm1Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;    // Set Immediate load
             EPwm1Regs.TBPRD = 750;                       // Period set for 400 kHz PWM
             hrDAC_period = 750;                          // Used for Q15 to Q0 scaling

             EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
             EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;      // EPWM1 is the Master
             EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
             EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
             EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;

          // Note: ChB is initialized here only for comparison purposes. It is not required

             EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
             EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
             EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // optional
             EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;   // optional

             EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
             EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
             EPwm1Regs.AQCTLB.bit.ZRO = AQ_SET;            // optional
             EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;          // optional
          // Now configure the HRPWM resources
             EALLOW;                                      // Note these registers are protected
                                                          // and act only on ChA.
             EPwm1Regs.HRCNFG.all = 0x0;                  // Clear all bits first
             EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP;       // Control falling edge position
             EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;       // CMPAHR controls the MEP.
             EPwm1Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;   // Shadow load on CTR=Zero.
             EDIS;
             MEP_ScaleFactor = 55*256;                    // Start with typical Scale Factor
                                                          // value for 300 MHz.
                                                          // Use SFO functions to update
                                                          // MEP_ScaleFactor dynamically.
}
```

Example 5 shows an assembly example of run-time code that can execute in a high-speed ISR loop.

Example 5. PWM DAC Function Run-Time Code

```
EPWM1_BASE   .set 0x6800
CMPAHR1      .set EPWM1_BASE+0x8

;================================================
HRPWM_DAC_DRV; (can execute within an ISR or loop)
;================================================
      MOVW DP, #_HRDAC_In
      MOVL XAR2,@_HRDAC_In              ; Pointer to input Q15 duty (XAR2)
      MOVL XAR3,#CMPAHR1                ; Pointer to HRPWM CMPA reg (XAR3)

; Output for EPWM1A (HRPWM)
      MOV T,*XAR2                       ; T <= duty
      MPY ACC,T,@_hrDAC_period          ; Q15 to Q0 scaling based on period
      ADD ACC,@_HrDAC_period<<15        ; Offset for bipolar operation
      MOV T,@_MEP_ScaleFactor           ; MEP scale factor (from optimizer s/w)
      MPYU P,T,@AL                      ; P <= T * AL, optimizer scaling
      MOVH @AL,P                        ; AL <= P, move result back to ACC
      ADD ACC, #0x180                   ; MEP range and rounding adjustment
      MOVL *XAR3,ACC                    ; CMPA:CMPAHR(31:8) <= ACC

; Output for EPWM1B (Regular Res) Optional - for comparison purpose only
      MOV *+XAR3[2],AH                  ; Store ACCH to regular CMPB
```

3 HRPWM Register Descriptions

This section describes the applicable HRPWM registers

3.1 Register Summary

A summary of the registers required for the HRPWM is shown in the table below.

Table 6. Register Descriptions

Name	Offset	Size (x16)	Description
Time Base Registers			
TBCTL	0x0000	1/0	Time Base Control Register
TBSTS	0x0001	1/0	Time Base Status Register
TBPHSHR	**TBPHSHR**	**1/0**	**Time Base Phase High Resolution Register**
TBPHS	0x0003	1/0	Time Base Phase Register
TBCNT	0x0004	1/0	Time Base Counter Register
TBPRD	0x0005	1/1	Time Base Period Register Set [3]
Reserved	0x0006	1/0	
Compare Registers			
CMPCTL	0x0007	1/0	Counter Compare Control Register
CMPAHR	**0x0008**	**1/1**	**Counter Compare A High Resolution Register Set**
CMPA	0x0009	1/1	Counter Compare A Register Set
CMPB	0x000A	1/1	Counter Compare B Register Set [4]
EPWM Registers			
ePWM	0x0000 to 0x001F	32	Other ePWM registers including the ones given above.
HRCNFG	**0x0020**	**1**	**HRPWM Configuration Register**
EPWM/HRPWM Test Registers			
Reserved	0x0030 0x003F	16	

3.2 Registers and Field Descriptions

Figure 12. HRPWM Configuration Register (HRCNFG)

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		HRLOAD	CTLMODE	EDGMODE	
R-0		R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. HRPWM Configuration Register (HRCNFG) Field Descriptions

Bit	Field	Value	Description [(1)]
15-4	Reserved		Reserved
3	HRLOAD		Shadow mode bit: Selects the time event that loads the CMPAHR shadow value into the active register:
		0	CTR = zero (counter equal zero)
		1	CTR=PRD (counter equal period)
			Note: Load mode selection is valid only if CTLMODE=0 has been selected (bit 2). You should select this event to match the selection of the CMPA load mode (i.e., CMPCTL[LOADMODE] bits) in the EPWM module as follows:
			00 Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000)
			01 Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD)
			10 Load on either CTR = Zero or CTR = PRD (should not be used with HRPWM)
			11 Freeze (no loads possible – should not be used with HRPWM)
2	CTLMODE		Control Mode Bits: Selects the register (CMP or TBPHS) that controls the MEP:
		0	CMPAHR(8) Register controls the edge position (i.e., this is duty control mode). (default on reset)
		1	TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode).
1-0	EDGMODE		Edge Mode Bits: Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic:
		00	HRPWM capability is disabled (default on reset)
		01	MEP control of rising edge
		10	MEP control of falling edge
		11	MEP control of both edges

(1) This register is EALLOW protected.

Figure 13. Counter Compare A High Resolution Register (CMPAHR)

15	8	7	0
CMPAHR		Reserved	
R/W-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. Counter Compare A High Resolution Register (CMPAHR) Field Descriptions

Bit	Field	Value	Description
15-8	CMPAHR		Compare A High Resolution register bits for MEP step control. A minimum value of 0x0001 is needed to enable HRPWM capabilities. Valid MEP range of operation is 1-255h.
7-0	Reserved		Any writes to these bit(s) must always have a value of 0.

Figure 14. TB Phase High Resolution Register (TBPHSHR)

15	8	7	0
TBPHSH		Reserved	
R/W-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. TB Phase High Resolution Register (TBPHSHR) Field Descriptions

Bit	Field	Value	Description
15-8	TBPHSH		Time base phase high resolution bits
7-0	Reserved		Any writes to these bit(s) must always have a value of 0.

Appendix A SFO Library Software - SFO_TI_Build_V5.lib

This appendix includes a detailed description of the software routines in SFO_TI_Build_V5.lib which supports up to 16 HRPWM channels.

A.1 SFO library Version Comparison

Table 10 includes a high-level comparison between SFO_TI_Build.lib and SFO_TI_V5.lib. A detailed description of SFO_TI_Build_V5.lib follows the table, and more information on SFO_TI_Build.lib can be found in Section 2.4.

Table 10. SFO library Version Comparison

	SYSCLK Freq	ePWM Freq	SFO_TI_Build.lib	SFO_TI_Build_V5.lib	Unit
Max. HRPWM channels supported	-	-	Up to 4	Up to 16	channels
Total static variable memory size	-	-	220	79(1 ch.) to 192 (16ch.)	words
MepEn runs on multiple channels concurrently?	-	-	yes	no	-
Error-checking?	-	-	no	yes	-
Typical time requires for MepEn to update	-	3.33 MHz	0.396	0.18	seconds
	-	400 kHz	3.26	1.5	seconds
MEP_ScaleFactor on 1 channel if called repetitvely without interrupts	-	1 MHz	1.308	0.6	seconds
	-	2 MHz	0.66	0.3	seconds
	-	20 MHz	0.066	0.03	seconds
Typical time required for MepDis to update	100MHz		0.83	0.83	milliseconds
MEP_ScaleFactor on 1 channel if called repetitively without interrupts	60MHz		1.38	1.38	milliseconds
	50MHz		1.66	1.66	milliseconds

In SFO_TI_Build_V5.lib/SFO_TI_Build_V5B.lib, the diagnostic software has been optimized to use less memory, to minimize the calibration time, and to support up to 16 HRPWM channels. Table 11 provides functional description of the two SFO library routines in SFO_TI_Build_V5.lib/SFO_TI_Build_V5B.lib.

NOTE: For the F2833x floating point devices, when compiling application code for floating point (fpu32 mode), libraries utilized by the application code must also be compiled for floating point. The SFO_TI_Build_fpu.lib and SFO_TI_Build_V5_fpu.lib are available as the floating point compiled equivalents to the fixed point SFO_TI_Build.lib and SFO_TI_Build_V5.lib libraries. The SFO functions in the fpu-version libraries are C-code-compatible to their fixed-point equivalents.

Table 11. SFO V5 Library Routines

Function	Description
int SFO_MepDis_V5(n)	**Scale Factor Optimizer V5 with MEP Disabled**
	This routine is very similar to the SFO_MepDis() routine in the original SFO library, but with one change. It now returns a 1 when MEP-disabled calibration is complete, or a 0 while calibration is still running. This function runs faster than the SFO_V5() routine and cannot be used on an ePWM channel while HRPWM capablities are enabled for that channel. If there is a spare ePWM channel availablein the system. SFO_MepDis_V5() can be run for that channel, and the resulting MEP_ScaleFactor[n] value can be copied into the MEP_ScaleFactor[n] for all other channels. If SYSCLKOUT = TBCLK = 300 MHz and assuming the MEP step size is 60 ps: Typical value at 300 MHz = 55 MEP steps per unit TBCLK (10 ns) The funtion returns a value in the variable array: MEP_ScaleFactor[n] Number of MEP steps/SYSCLKOUT If TBCLK is not equal to SYSCLKOUT, then the returned value must be adjusted to reflect the correct TBCLK: MEP steps per TBCLKK =MEP_ScaleFactor[n] * (SYSCLKOUT/TBCLK) Example: If TBCLK = SYSCLKOUT/2, MEP steps per TBCLK = MEP_ScaleFactor[n] * (300/150) = 55 *2 = 110 **Constraints when using this function:** • SFO_MepDis_V5(n) can be used with SYSCLKOUT from 200 MHz to maximum SYSCLK frequency. MEP diagnostics logic uses SYSCLKOUT and not TBCLK. Hence, the SYSCLKOUT restriction is an important constraint. • If TBCLK does not equal SYSCLKOUT, the TBCLK frequency must be great enough so that MEP steps per TBCLK do not exceed 255. This is due to the restriction that there can be no more than 255 MEP steps in a coarse step. For this reason it is highly recommended that TBCLK=SYSCLKOUT. • This function cannot be run on an ePWM channel with HRPWM capabilities enabled. Running the SFO_MepDis_V5 function continuously in an application will generate an inaccurate waveform on the HRPWM channel output pin. **Usage:** • If one of the ePWM modules is running in normal ePWM mode, then it can be used to run the SFO diagnostics function. Here, the single MEP_ScaleFactor value obtained for that channel can be copied and used as the MEP_ScaleFactor for the other ePWM modules which are running HRPWM modules' MEP steps are similar but may not be identical. • This routine returns a 1 when calibration is finished on the specified channel or a 0 if calibration is still running. • The ePWM module that is not active in HRPWM mode is still fully operational in conventional PWM mode and used to drive PWM pins. The SFO function only makes use of the MEP diagnostics logic in the HRPWM circuitry. • SFO_MepDis_V5(n) function does not require a starting Scale Factor value. • The other ePWM modules operating in HRPWM mode incur only a 3-cycle minimum duty cycle limitation.
int SFO_MepEn_V5(n)	**Scale Factor Optimizer V5 with MEP Enabled**
	This function runs slower that the SFO_MepDis_V5() routine and runs SFO diagnostics on an ePWM channel with HRPWM capabilities enabled for that channel. If SYSCLK = TBCLK = 300 MHz, and assuming MEP step size is 60 ps: Typical value at 300 MHz = 55 MEP steps per unit TBCLK (3.33 ns) The function returns a value in the variable array: MEP_ScaleFactor(n) =Number of MEP steps/SYSCLKOUT =Number of MEP steps/TBCLK

Table 11. SFO V5 Library Routines (continued)

Function	Description
	Constraints when using this function:
	• This routine must be run on one channel at a time and cannot be run on multiple channels concurrently. When it has finished updating the MEP_ScaleFactor for a channel, it will return a 1. If it is still calibrating, it will return a 0. A background loop should exist in the ISR code which calls SFO_MepEn_V5(n) repeatedly until it returns a 1. Then the function can be called for the next channel.[(1)]
	NOTE: Unlike the original SFO_MepEn(n) routine, this routine cannot run on multiple channels concurrently. Do not call SFO_MepEn_V5(n) for another channel until the function returns a 1 for the current channel. Otherwise, the MEP_ScaleFactor for both channels will become corrupted.
	NOTE: SFO_MepEn_V5(n) in SFO_TI_Build_V5.lib supports only the following HRPWM configuration: • HRCNFG[HRLOAD] = 0 (load on CTR = ZERO) • HRCNFG[EDGMODE] = 10(falling edge MEP control) An upgraded version of SFO_MepEn_V5(n) in SFO_TI_Build_V5B.lib supports all available HRPWM configurations. When using this version, the HRCNFG register must be initialized with the appropriate configuration after calling SFO_MepDis_V5(n) to seed the MEP_ScaleFactor[n] and prior to calling SFO_MepEn_V5(n).
	• The SFO_MepEn_V5(n) function requires a SYSCLKOUT between 200 MHz and 300 MHz (or maximum SYSCLK frequency) only. MEP diagnostics logic uses SYSCLKOUT and not TBCLK. Hence the SYSCLKOUT restriction is an important constraint. It is highly recommended that TBCLK=SYSCLKOUT.
	Usage:
	• After calling SFO_MepDis(n) to seed MEP_ScaleFactor[n], and prior to using the SFO_MepEn(n) function in SPO_TI_Build_V5B.lib, the HRCNFG register must be initialized with the desired HRPWM configuration. Otherwise, calibration will not be initiated, and calls to SFO_MepEn_V5(n) will continuously return 0. • The SFO_MepEn_V5(n) function requires a starting scale factor value, MEP_ScaleFactor[0]. MEP_ScaleFactor[0] needs to be initialized to a typical MEP step size value. To do this, SFO_MepDis_V5(n) can be run on an ePWM channel while the HRPWM is disabled, and the resulting MEP_ScaleFactor[n] value can be copied into MEP_ScaleFactor[0]. • If there are drastic environmental changes to your system (i.e. temperature/voltage), it is generally a good idea to re-seed MEP_ScaleFactor[0] with a new typical MEP step size value for the changed conditions. • Because SFO_MepEn_V5(n) can be run on only one channel at a time, it is only recommended for systems where there are no spare HRPWM channels available, so SFO calibration must be performed on all channels with HRPWM capabilities enabled. In this case, a 6-cycle MEP inactivity zone exists at the start of each PWM period on all HRPWM channels. See Section 2.3.3 on duty cycle range limitations. • The function returns: – A one when it has finished SFO calibration for the current channel – A zero when SFO diagnostics are still running for the channel – A two as an error indicator after calibration has completed if the resulting MEP_ScaleFactor for the channel differs from the original MEP_ScaleFactor[0] seed value by more than +/- 15
	The function must be called repetitively before it will return a 1. This function takes a longer time to complete than the SFO_MepDis_V5(n) calibration.

(1) If SFO calibration must be run on multiple channels at a time while HRPWM capabilities are enabled, the previous version of the SFO library, SFO_TI_Build.lib, which uses more memory resources, can be used instead, and SFO_MepEn(n) can run concurrently for up to 4 ePWM channels with HRPWM enabled.

Table 11. SFO V5 Library Routines (continued)

Function	Description
	If it returns a 2, the MEP_ScaleFactor for the channel has finished updating and is outside the typical drift range of MEP_ScaleFactor[0] +/- 15 even with large temperature and voltage variations. If the reason for large difference between the seed and the channel scale factor is known and acceptable, the user may choose to ignore the return value of 2, and treat it as a return value of 1, indicating that calibration is complete. Otherwise, if the large difference is unexpected, there are steps to take to remedy the error: 1. Check your code to ensure SFO_MepEn_V5(n) is not being called on more than one channel at a time. 2. If the above is not effective, run SFO_MepDis_V5(n) again and re-seed Mep_ScaleFactor[0]. 3. If neither of the above 2 steps work, there may be a system problem. The application firmware should perform shutdown or an appropriate recovery procedure. • If all ePWM modules are using the same TBCLK prescalers, it is possible to run the SFO_MepEn_V5(n) function for only one ePWM module and to use the MEP_ScaleFactor value for that module for the other modules also. In this case only one ePWM module incurs the 6-cycle duty limitation, and the remaining modules incur only a 3-cycle minimum duty limitation. This assumes that all HRPWM modules' MEP steps are similar but may not be identical.

A.2 Software Usage

Software library functions int SFO_MepEn_V5(int n) and int SFO_MepDis_V5(int n) calculate the MEP scale factor for ePWMn Modules, where n= the ePWM channel number. The scale factor value, which represents the number of micro-steps availablein a system clock period, is returned in a global array of integer values called MEP_ScaleFactor[x], where x is he maximum numver of HRPWM channels for a device plus one. For example, if the maximum number of HRPWM channels for a device is 16, the scale factor array would be MEP_ScaleFactor[17]. Both SFO_MepEn_V5 and SFO_MepDis_V5 themselves also return a 1 when calibration has completed, indicating the MEP_ScaleFactor has been successfully updated for the channel, and a 0 when calibration is still on-going. A return of 2 represents an out-of-range error.

Table 12. Software Functions

Software functional calls	Functional Description
int SFO_MepDis_V5(int n) (1)	
status = SFO_MepDis_V5(1)	The scale factor in MEP_ScaleFactor[1] updated when status = 1.
status = SFO_MepDis_V5(2)	The scale factor in MEP_ScaleFactor[2] updated when status = 1.
...	...
status = SFO_MepDis_V5(16)	The scale factor in MEP_ScaleFactor[16] updated when status = 1 or 2.
int SFO_MepEn_V5(int n) (1)	
status = SFO_MepEn_V5(1)	The scale factor in MEP_ScaleFactor[1] updated when status = 1 or 2.
status = SFO_MepEn_V5(2)	The scale factor in MEP_ScaleFactor[2] updated when status = 1 or 2.
...	...
status = SFO_MepEn_V5(16)	The scale factor in MEP_ScaleFactor[16] updated when status = 1 or 2.

(1) MEP_ScaleFactor[0] is a starting seed value used by the SFO software functions internally.

To use the HRPWM feature of the ePWMs, it is recommended that the SFO functions in TI_Build_V5.lib be used as described here. The examples below are specific to the TMS320C28346 device, which includes a maximum of 9 HRPWM channels. For different devices which may have fewer HRPWM channels, modifications will be required in Step 1 and Step 2 below.

Step 1. Add "Include" Files

The SFO_V5.h file needs to be included as follows. This include file is mandatory when using the SFO V5 library functions. For the TMS320C28346 device, the C2834x C/C++ Header Files and Peripheral Examples DSP2834x_Device.h and DSP2834x_PWM_defines.h files are necessary as will, as they are used by all TI software examples for the device. These file names will change in accordance with your specific device. These include files are optional if customized header files are used in the end application. See example below.

Example 1. A Sample of How to Add "Include" Files

```
#include "DSP2834x_Device.h"         //DSP2834x Headerfile
#include "DSP2834x_EPWM_defines.h"   //init defines
#include "SFO_V5.h"                  //SFO V5 lib functions (needed for HRPWM)
```

Step 2. Define Number of HRPWM Channels Used

In the SFO_V5.h file, the maximum number of HRPWM's used for a peticular device must be defines. PWM_CH must equal the number of HRPWM channels plus one. For instance, for the TMS320C28346 where there are 9 possible HRPWM channels, PWM_CH can be set to 10. For the TMS320C28342, where there are 6 possible HRPWM channnels, PWM_CH can be set to 7. See example below.

To save static variable memory, fewer than the maximum number of HRPWM channels may be defined with some caution. To do this, PWM_CH can be set to the largest ePWM channel number plus one. For instance, if only ePWM1A and ePWM2A channels are required as HRPWM channels, PWM_CH can be set to 3. However, if only ePWM8A and ePWM9A channels are required as HRPWM channels, PWM_CH must still be set to 10.

Example 2. Defining Number of HRPWM Channels Used (Plus One)

```
//SFO_V5.H
//NOTE: THIS IS A VERY IMPORTANT STEP> PWM_CH MUST BE DEFINED FIRST BEFORE
//BUILDING CODE

#define PWM_CH 10
                     //C28346 has a maximum of 9 HRPWM channels (10=9+1)
                     //For a device with maximum of 6 HRPWM channels, PWM_CH = 7
                     //For a device with maximum of 4 HRPWM channels, PWM_CH = 5
                     //For a device with maximum of 3 HRPWM channels, PWM_CH = 4
```

Step 3. Element Declaration

Declare an array of integer variables with a length equal to PWM_CH, and an array of pointers to EPWM register structures. The array of pointers will include pointers for up to 9 EPWM register structures plus one dummy pointer in location EPWM[0] for a device with 9 EPWM channels. Likewise, it will include pointers for up to 3 EPWM register structures plus one for a device with 3 EPWM registers.

Example 3. Declaring Elements Required by SFO_TI_Build_V5.lib

```
int MEP_ScaleFactor[PWM_Ch] = {0,0,0,0,0,  //Scale factor values for ePWM 1-9
                               0,0,0,0,0}; //and MEP_ScaleFactor[0]
                                           //For Fewer HRPWM channels, these
                                           //will be fewer zeros initialized

//Declare a volatile array of pointers to EPWM register structures.
//Only point to registers that exist. If a device has only 6 EPWMs (PWM_CH is 7),
//the array will include pointers for up to 6 EPWM register structures plus one
//dummy pointer in the ePWM[0] location.
volatile struct EPWM_REGS *ePWM[PWM_CH] {0, &EPwm1Regs &EPwm2Regs, &EPwm3Regs, &EPwm4Regs,
&EPwm5Regs, &EPwm6Regs, &EPwm7Regs,
&EPwm8Regs, &EPwm9Regs};
```

Step 4. MEP_ScaleFactor

After power up, the SFO_MepEn_V5(n) function needs a typical scale factor starting seed value in MEP_ScaleFacter[0]. This value can be conveniently determined using one of the ePWM modules to run the SFO_MepDis_V5(n) function prior to initializing the PWM settings for the application. The SFO_MepDis_V5(n) function does not require a starting scale factor value.

As part of the one-time initialization code prior to using MEP_ScaleFactor, include the following:

Example 4. Initializing With a Scale Factor Value

```
//MEP_ScaleFactor varaibles initialized using function SFO_MepDis_V5
Uint16 i;
for(i=1; i<PWM_CH; i++)             //for channels 1-9
{
        while (SFO_MepDis_V5(i) == 0){}  //Calls MepDis unitl MEP_ScaleFactor updated
}
//initialize MEP_ScaleFactor[0] with a typical MEP seed value
//required for SFO_MepEn_V5
    MEP_ScaleFactor[0] = MEP_ScaleFactor[1];
```

Step 5. Application Code

While the application is running, fluctuations in both device temperature and supply voltage may be expected. To be sure that optimal scalee factors are used for each ePWM modules, the SFO function should be re-run periodically as part of a slower background loop. Some examples of this are shown here in the below example.

Example 5. SFO Function Calls

```
main()
{
Uint16 current_ch = 1;         //keeps track of current HRPWM channel being calibrated
Uint16 status;

//user code

//Case 1: all ePWMs are running in HRPWM mode
//        here, the minimum duty cycle limitation is 6 clock cycles
    status = SFO_MepEn_V5(current_ch); //MepEn called here
    if(status == 1)                    //if MEP_ScaleFactor has been updated
{
          current_ch++;                //move on to the next channel
}
else if( status == 2)                  //if MEP_ScaleFactor differs from
{                                      //MEP_ScaleFactor[0] seed by more than
         error();                      //+/-15, flag an error
}
if(current_ch == PWM_CH)               //if last channel has been reached
{
        current_ch=1;                  //go back to channel 1
}

//Case 2: All ePWMs except one are running in HRPWM mode.
// One of the ePWM channels (ePWM9 in this example is used
// for SFO_MepDis_V5 scale factor calibration.
// Here, the minimum duty cycle limitation is 3 clock cycles.

// HRPWM diagnostics circuitry is used to estimate the MEP steps
// with the assumption that all HRPWM channels behave similarly
// though they may not be identical

        while( SFO_MepDis_V5(9) == 0); //wait until MEP_ScaleFactor[9] updates
        for(i=1; i<(PWM_CH-1); i++) //update scale factors for ePWM 1-9
```

```
        {
            MEP_ScaleFactor[i] = MEP_ScaleFactor[9];
        }
```

NOTE: See the hrpwm_sfo_v5 example in your device-specific Header Files and Peripheral Examples software package available on the TI website.

Appendix B Revision History

This document was revised and lists only revisions made in this most recent version. The scope of the revisions was limited to technical changes as shown in Table 13.

Table 13. Technical Changes in the Current Revision

Location	Additions, Deletions, Modifications
Global	**Replaced Map with Mep**
Global	Replaced MEP_SF to MEP_ScaleFactor
Section 1	Revised "Table values assume a MEP step size of 180 ps" to " These values assume a 100 MHz SYSCLK frequency and a MEP step size of 180 ps."
Figure 2	Revised 16-bit CMPAHR register value = ...
	Revised Note: For MEP range and rounding adjustment to include "(0x0180 in Q8 format)"
Figure 4	Changed TBCTL[CNTLDE] to TBCTL[PHSEN]
Section 2.3.1	Changed 180 ns to 180 ps
Section 2.3.2	Revised the **Assumptions for this example** section

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connctivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265