Benefits of a multiphase buck converter

By David Baba
Applications Engineering Manager

Introduction

Single-phase buck controllers work well for low-voltage converter applications with currents of up to approximately 25 A, but power dissipation and efficiency start to become an issue at higher currents. One suitable approach is to use a multiphase buck controller. This article briefly discusses the benefits of using a multiphase buck converter versus a single-phase converter and the value a multiphase buck converter can provide when implemented.

Figure 1 shows a two-phase circuit. From this circuit's waveforms, shown in Figure 2, it is clear that the phases are interleaved. Interleaving reduces ripple currents at the input and output. It also reduces hot spots on a printed circuit board or a particular component. In effect, a two-phase buck converter reduces the RMS-current power dissipation in the FETs and inductors by half. Interleaving also reduces transitional losses.

Figure 1. Two-phase buck converter

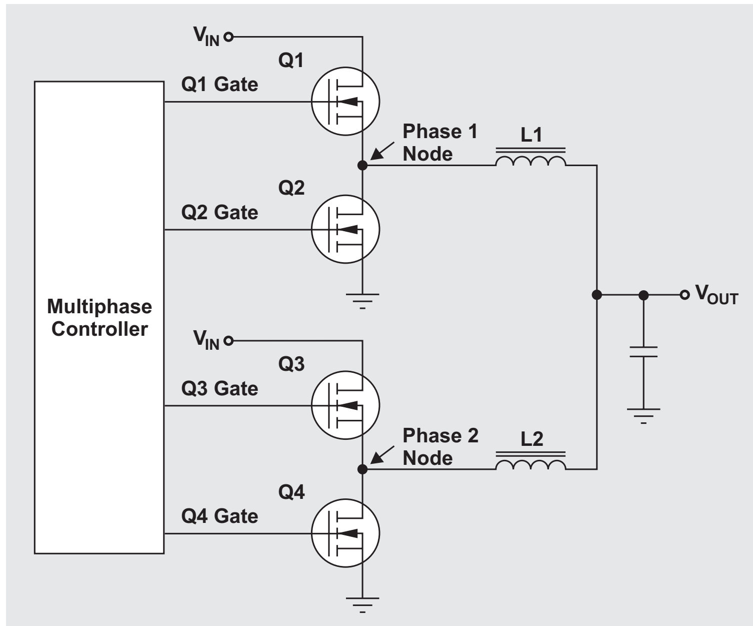
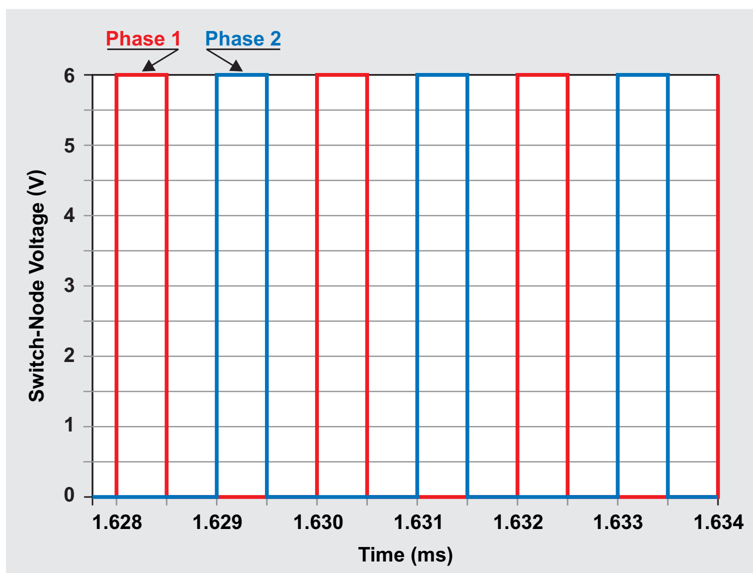


Figure 2. Node waveforms of phases 1 and 2



Output-filter consideration

The output-filter requirements decrease in a multiphase implementation due to the reduced current in the power stage for each phase. For a 40-A, two-phase solution, an average current of only 20 A is delivered to each inductor. Compared to a 40-A single-phase approach, the inductance and inductor size are drastically reduced because of lower average current and lower saturation current.

Output ripple voltage

Ripple-current cancellation in the output-filter stage results in a reduced ripple voltage across the output capacitor compared to a single-phase converter. This is another reason why a multiphase converter is preferred. Equations 1 and 2 calculate the percentage of ripple current canceled in each inductor.

$$m = D \times \text{Phases} \tag{1}$$

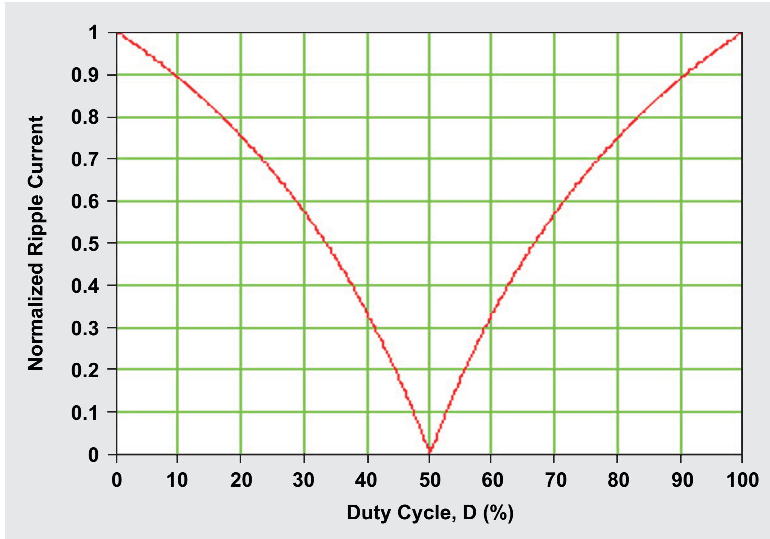
and

$$I_{\text{Rip\_norm}}(D) = \text{Phases} \times \frac{\left[D - \dfrac{mp(D)}{\text{Phases}}\right] \times \left[\dfrac{1 + mp(D)}{\text{Phases}} - D\right]}{(1-D) \times D}, \tag{2}$$

where D is the duty cycle, I_{Rip_norm} is the normalized ripple current as a function of D, and mp is the integer of m. Figure 3 plots these equations. For example, using two phases at a 20% duty cycle (D) yields a 25% reduction in ripple current. The amount of ripple voltage the capacitor must tolerate is calculated by multiplying the ripple current by the capacitor's equivalent series resistance. Clearly, both maximum current and voltage requirements are reduced.

Figure 4 shows the simulation results for a two-phase buck converter at a duty cycle of 25%. The inductor ripple current is 2.2 A, but the output capacitor sees only 1.5 A due to ripple-current cancellation. With a duty cycle of 50% and two phases, the capacitor sees no ripple current at all.

Figure 3. Normalized capacitor ripple current as a function of duty cycle



Load-transient performance

Load-transient performance is improved due to the reduction of energy stored in each output inductor. The reduction in ripple voltage as a result of current cancellation contributes to minimal output-voltage overshoot and undershoot because many cycles will pass before the loop responds. The lower the ripple current is, the less the perturbation will be.

Cancellation of input RMS ripple current

The input capacitors supply all the input current to the buck converter if the input wire to the converter is inductive. These capacitors should be carefully selected to satisfy the RMS-ripple-current requirements to ensure that they

Figure 4. Cancellation of inductor ripple current with D = 25%

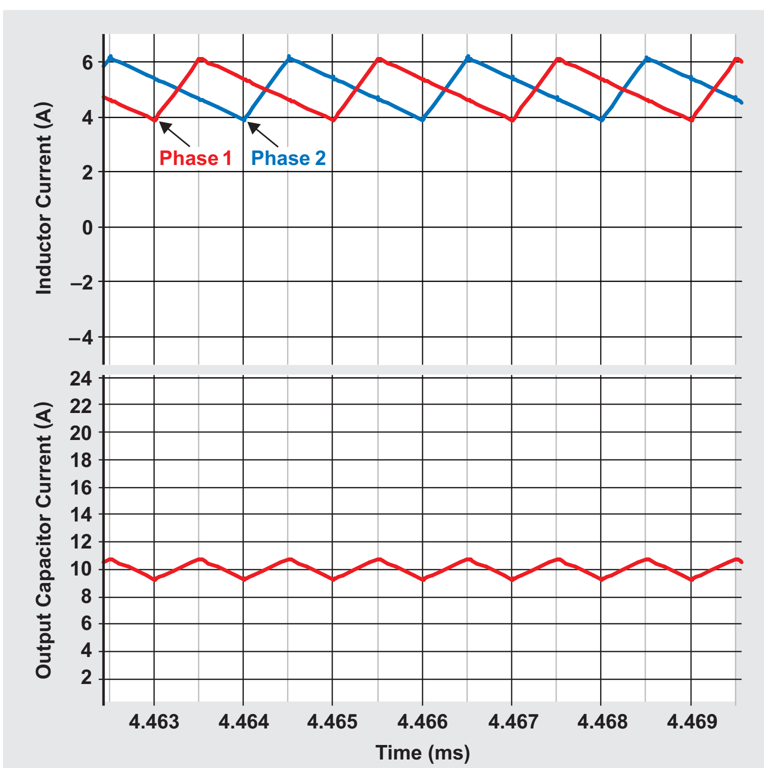


Figure 5. Normalized input RMS ripple current as a function of duty cycle

do not overheat. It is well understood that, for a single-phase converter with a duty cycle of 50%, the worst-case input RMS ripple current is typically rated at 50% of the output current. Figure 5 and Equation 3 indicate that, for a two-phase solution, the worst-case RMS ripple current occurs at duty cycles of 25 and 75% and is only 25% of the output current.

$$I_{Input\_norm}(D) = \sqrt{\left[D - \frac{mp(D)}{Phases}\right] \times \left[\frac{mp(D)+1}{Phases} - D\right]} \quad (3)$$

The value of a multiphase solution as compared to a single-phase solution is clear. Less input capacitance can be used to satisfy the RMS-ripple-current demands of the buck stage.

Table 1. Operating conditions of LM3754 evaluation board

Input voltage	10.8 to 13.2 V
Output voltage	1.2 V ± 1%
Output current	40 A (max)
Switching frequency	300 kHz
Module size	2 × 2 inches
Circuit area	1.4 × 1.3 inches
Module height	0.5 inches
Air flow	200 LFM
Number of phases	2

Application example

The LM3754 high-power-density evaluation board delivers 1.2 V at 40 A from a 12-V input supply. The board is 2 × 2 inches, and the area covered by the components is 1.4 × 1.3 inches. The switching frequency of each phase is set to 300 kHz. Table 1 provides a summary of these and other operating conditions. The components are placed on a 4-layer board, with 1 oz. of copper on all layers. Additional pins are included on this board for remote sensing, and a pin is used for margining the output voltage.

Because the LM3754 evaluation board is designed to operate in high-power-density configurations, it utilizes the optimized input capacitors to provide the reduced RMS ripple current that is required. The evaluation board also has a low ripple voltage and good transient performance. The board layout shown in the LM3754 application note[1] should be followed as closely as possible. However, if this is not possible, close attention should be paid to these considerations. Several more layout considerations will now be described, followed by the test results from a test board using the LM3754. These results are presented in Figures 6–11 on pages 12–13. They are typical of what one can expect to achieve or even improve upon in making the necessary modifications.

Layout considerations

High-current traces require enough copper to minimize voltage drops and temperature rises. The general rule of using a minimum of 7 mils per ampere was applied for the 2 oz. of copper used, and 14 mils per ampere for the inner layers for the 1 oz. of copper used. The input capacitors of each phase were placed as close as possible to the top MOSFET drain and the bottom MOSFET source to ensure minimal ground "bounce."

Signal components connected to the IC

All small-signal components that connected to the IC were placed as close to it as possible. Decoupling capacitors for V_{REF} and V_{CC} were also placed as close as possible to the IC. The signal ground (SGND) was configured to ensure a low-impedance path from the ground of the signal components to the ground of the IC.

SGND and PGND connections

Good layout techniques include a dedicated ground plane; this board dedicated as much of inner-layer 2 as possible for the ground plane. Vias and signal lines were strategically placed to avoid high-impedance points that could pinch off wide copper areas. The power ground (PGND) and SGND were kept separate, only connected to each other at the ground plane (inner layer 2).

Gate drive

The designer should ensure that a differential pair of traces is connected from the high-gate output to the top MOSFET gate and the return, which is the switch node. The distance between the controller and the MOSFET should be as short as possible. The same procedure should be followed for the LG and GND pins when the traces for the low-side MOSFET are routed.

A differential pair of traces must also be routed from the CSM and CS2 pins to the RC network located across the output inductor. Notice in the layout in Reference 1 that, in order to provide additional noise suppression, the filter capacitor is split into two capacitors—one positioned by the inductor and the other close to the IC. These sense lines should not be run for long lengths in close proximity to the switch node. If possible, they should be shielded by using a ground plane.

Minimizing the switch node

To follow the common rules of keeping the switch-node area as small as possible but large enough to carry high currents, the switch node was built on multiple layers. Because the small evaluation board essentially folds back on itself from input to output, the switch node naturally sits on the outer layer, and the IC sits directly underneath the switch node. Therefore, it is essential to keep the switch node well away from the sense lines and also from the IC. Hence, the switch node was strategically placed facing outwards toward the edge of the board.

Conclusion

There are a number of benefits to using multiphase buck converters, such as higher efficiency from lower transitional losses; lower output ripple voltage; better transient performance; and lower ripple-current-rating requirements for the input capacitor. Some examples of multiphase buck converters that can deliver the full benefits described herein are the LM3754, LM5119, and LM25119 families.

Reference

1. Robert Sheehan and Michael Null, "LM3753/54 evaluation board," National Semiconductor Corp., Application Note 2021, Dec. 15, 2009 [Online]. Available: http://www.national.com/an/AN/AN-2021.pdf

Related Web sites

power.ti.com
www.ti.com/product/*partnumber*
Replace *partnumber* with LM3754, LM5119, or LM25119

Test results

Figure 6. Efficiency plot with 12-V input

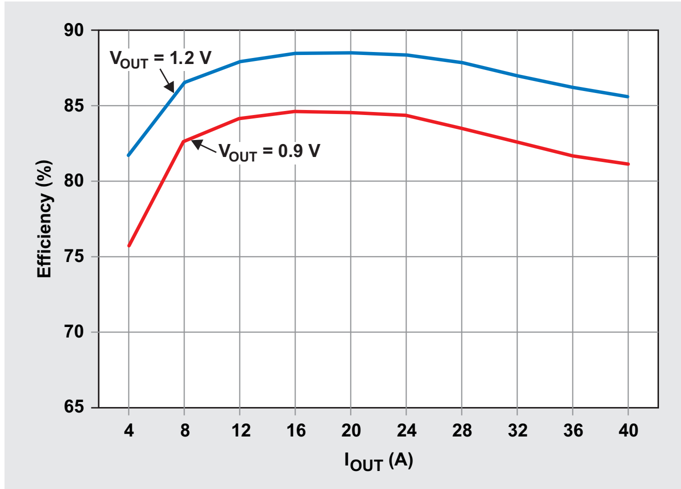


Figure 7. Power loss with 12-V input

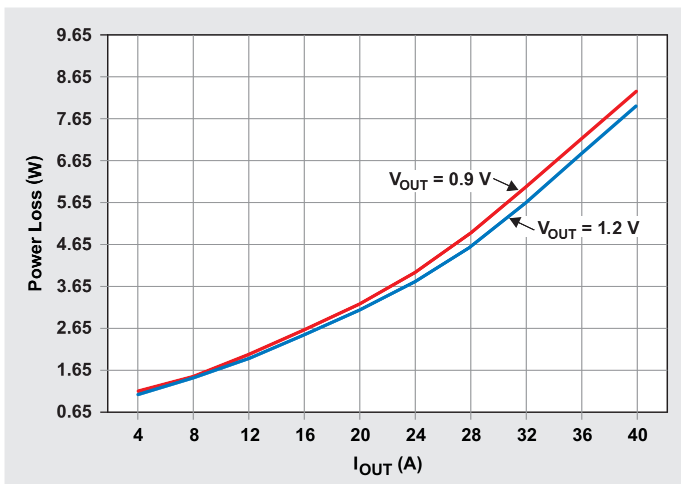
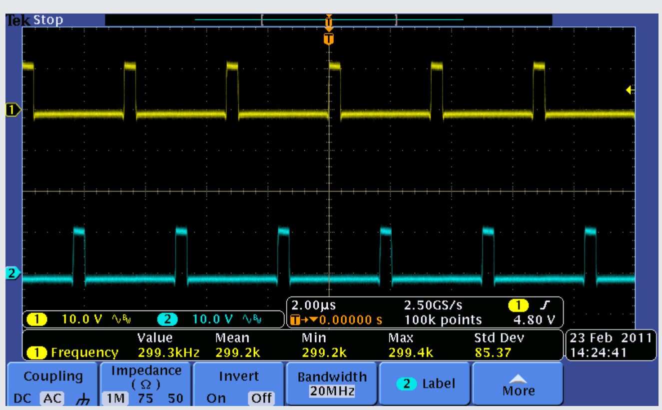
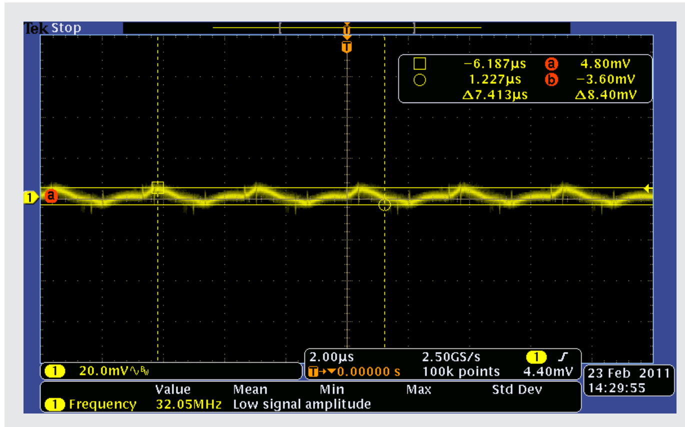


Figure 8. Switch-node voltages



V_{IN} = 12 V, V_{OUT} = 1.2 V at 40 A

Figure 9. Output voltage ripple



V_{IN} = 12 V, V_{OUT} = 1.2 V at 40 A

Figure 10. Transient response: 20 µs with 10-A load step (undershoot/overshoot ~ 27 mV)

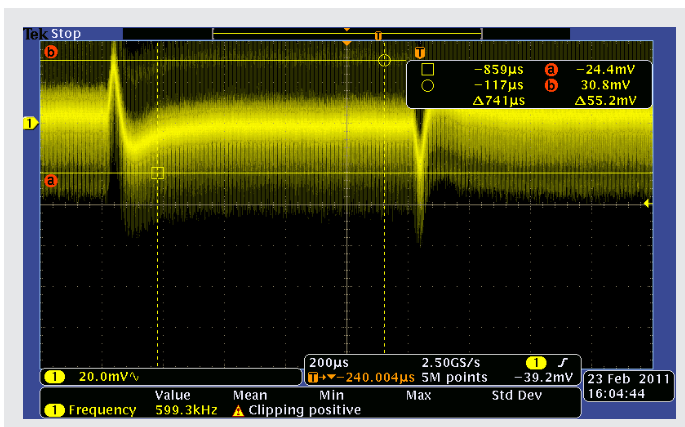
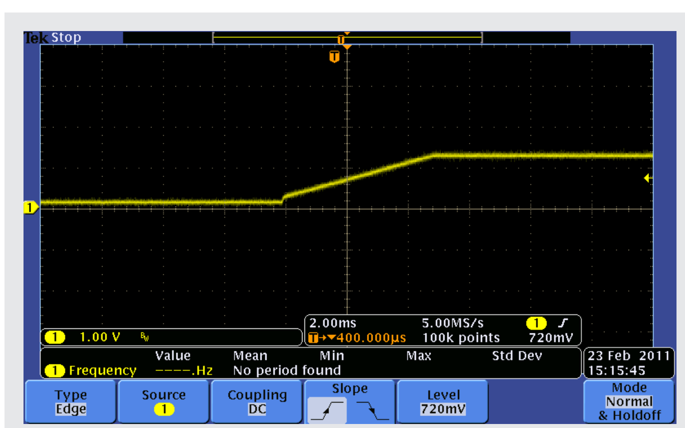


Figure 11. V_{OUT} start-up for 1.2-V output with 40-A load



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