Application Report
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Designing With MSP430F522x and MSP430F521x Devices

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ABSTRACT

The MSP430F522x and MSP430F521x devices support a split supply I/O system that is essential in systems in which the MCU is required to interface with external devices (such as sensors or other processors) that operate at different voltage level compared to the MCU device supply. Additionally, the split supply input voltage range of the F522x and F521x devices starts as low as 1.62 V (see the device data sheet specifications), and this allows for nominal 1.8-V I/O interface without the need for external level translation. This application report describes the various design considerations to keep in mind while designing the F522x and F521x devices in an application.

The application report discusses the new features of F522x and F521x devices, which mainly include the split-supply I/O system and the various digital functions supplied from the split-supply I/O rail.

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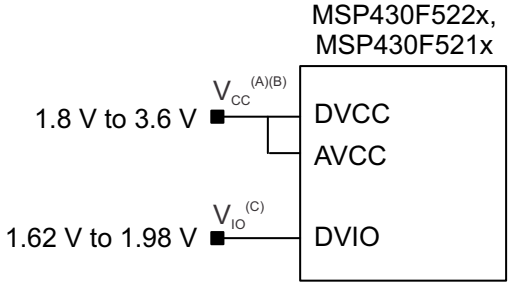
1 Split-Supply I/O Systems

For split-supply I/O systems, the split supplies are connected to the V_{CC} (DVCC and AVCC) and DVIO pins. Supply voltage at DVCC and AVCC pins (V_{CC}) is used to provide device power, and the supply voltage at the DVIO pin (V_{IO}) is used to supply the I/O rail of the "DVIO supplied I/O pins". The recommended V_{CC} supply voltage ranges from 1.8 V to 3.6 V (see note A on Figure 1) and, therefore, these devices do not operate at nominal 1.8 V (that is, 1.8 V ± 10%) supply voltage level. The V_{IO} supply voltage ranges from 1.62 V to V_{CC} and is useful in applications that interface with nominal 1.8-V I/O interface (that is, 1.8 V ± 10%).



A The recommended V_{CC} supply voltage range of 1.8 V to 3.6 V is applicable to the V_{CORE} setting of PMMCOREVx = 0. See the device data sheet for the V_{CC} supply voltage ranges at different V_{CORE} settings.

B It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power-up and operation.

C See the MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers data sheet for the V_{IO} supply voltage range.

Figure 1. Split Supply I/O Systems

2 DVIO Supplied I/Os

A group of general-purpose I/Os reside on the DVIO supply domain and are called DVIO supplied I/Os. On the MSP430F522x devices, the following I/Os reside on the DVIO supply domain: Port1 (P1.4 to P1.7), Port2, Port3, Port4, and Port7. The remaining port I/Os reside on the DVCC supply domain.

In the data sheet, these I/O ports are highlighted in the functional block diagrams and are also pointed out in the signal descriptions table for respective I/O pins. Also, the electrical characteristics of I/Os in the DVIO and the DVCC domains are specified separately in MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers.

3 Secondary Digital Functions on DVIO Supplied I/Os

The DVIO supplied general-purpose I/Os are multiplexed with other digital functions in the device, and these digital functions' I/O circuits are also powered from DVIO. On the F522x and F521x devices, some of the secondary digital functions that are shared with the DVIO supplied I/Os include timer capture compare functions, serial communication functions (USCI UART, SPI, or I^2C), comparator output, SMCLK output, and MCLK output. See the signal descriptions table in MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers for details.

On the F522x and F521x devices, Port 4 supports port mapping and resides on the DVIO supply domain. Any of the secondary digital functions specified in the port mapping table can be mapped to Port4, and their respective I/O circuitry is supplied by DVIO. See the port mapping table in the *Peripherals* section of the data sheet for details.

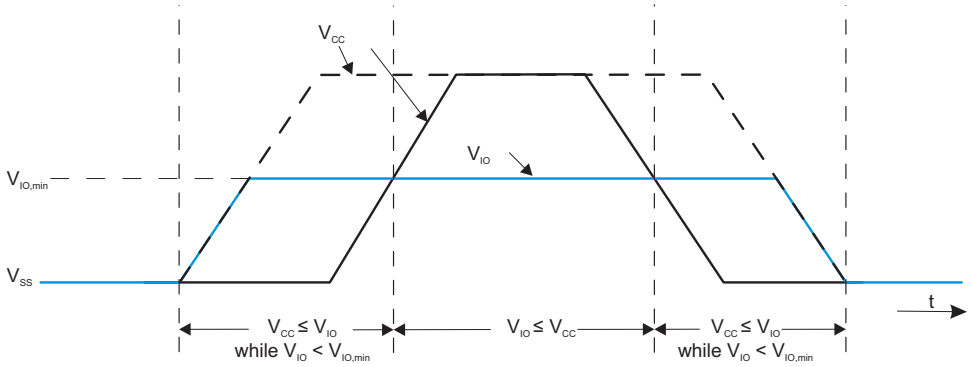
NOTE: In split supply I/O systems, if external pullup resistors are connected to any of the DVIO supplied pins (for example, the USCI I^2C pins – SDA and SCL), tie the external pullups to the DVIO supply and not to DVCC.

Other DVIO supplied digital pins on the F522x and F521x devices include:

- BSLEN – BSL enable pin used by the DVIO supplied BSL interface (see Section 7). By default, this pin has a nonconfigurable internal pulldown resistor enabled.
- $\overline{\text{RST}}$/NMI – DVIO supplied reset pin multiplexed with NMI functionality. See Section 5 for details of the reset functionality.

4 Split-Supply Power-Up or Power-Down Sequence

For split-supply I/O systems, it is required that the $V_{IO} \geq V_{CC}$ during the ramp up phase of V_{IO} and V_{CC}. During V_{CC} and V_{IO} power down, it is required that $V_{IO} \geq V_{CC}$ during the ramp down phase of V_{IO} and V_{CC}. Figure 2 is an excerpt from the data sheet.



NOTE: The device supports continuous operation with $V_{CC} = V_{SS}$ while V_{IO} is fully within its specification. During this time, the general-purpose I/Os that reside on the V_{IO} supply domain are configured as inputs and pulled down to V_{SS} through their internal pulldown resistors. $\overline{\text{RST}}$/NMI is high impedance. BSLEN is configured as an input and is pulled down to V_{SS} through its internal pulldown resistor. When V_{CC} reaches above the BOR threshold, the general-purpose I/Os become high-impedance inputs (no pullup or pulldown enabled), $\overline{\text{RST}}$/NMI becomes an input pulled up to V_{IO} through its internal pullup resistor, and BSLEN remains pulled down to V_{SS} through its internal pulldown resistor.

Figure 2. V_{CC} and V_{IO} Power Sequencing

5 Reset and NMI Pin Functionality

On the F522x and F521x devices, there are two reset pins:

- $\overline{\text{RSTDVCC}}$/SBWTDIO: resides on the DVCC supply domain
- $\overline{\text{RST}}$/NMI: resides on the DVIO supply domain

The device can be held in reset by asserting a low on either of the two reset pins. However, the NMI pin functionality is available only on the $\overline{\text{RST}}$/NMI pin and is not multiplexed with the $\overline{\text{RSTDVCC}}$ pin.

The $\overline{\text{RSTDVCC}}$ pin has an internal pullup that is always enabled and is not configurable. The $\overline{\text{RST}}$/NMI pin has configurable internal pullup and pulldown resistors available. By default, the internal pullup resistor on the $\overline{\text{RST}}$/NMI pin is enabled. The SYSRSTUP and SYSRSTRE bits in the reset pin control register (SFRRPCR) are used to select either the internal pullup or pulldown and to enable them, respectively.

If the $\overline{\text{RST}}$/NMI pin is unused, select and enable the internal pullup resistor, or connect an external pullup resistor (47 kΩ recommended) to the pin.

NOTE: Because all of the 4-wire JTAG pins (on Port J) reside on the DVCC supply domain, use the $\overline{\text{RSTDVCC}}$ pin which also resides on the DVCC supply domain for the JTAG interface and not the DVIO supplied $\overline{\text{RST}}$/NMI pin. For more details, see the JTAG pin requirements and functions table in MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers.

6 XT1 and XT2 Oscillators in Bypass Mode

The F522x and F521x devices have two on-chip crystal oscillators:

- XT1: low-frequency crystal oscillator
- XT2: high-frequency crystal oscillator

Both XT1 and XT2 oscillators can be operated in crystal bypass mode, in which external clock signals are input to the XIN and XT2IN pins, respectively, and the oscillators associated with XT1 and XT2, respectively, are powered down. By default, the XIN and XT2IN pins reside on the DVCC supply domain and require the external clock signal to meet the data sheet specified input specifications for I/Os in DVCC domain.

Additionally, the F522x and F521x devices support XT1 and XT2 bypass operation with external clock inputs that reside on the DVIO supply domain. Setting the XT1BYPASSLV and XT2BYPASSLV bits in the UCSCTL9 register enables the XT1 and XT2 bypass operations, respectively, with external clock signals that swing from 0 V to DVIO.

In both the cases, the external clock input frequency must meet the data sheet parameters for the chosen mode.

On the F522x and F521x devices, the XIN and XOUT (XT1) and XT2IN and XT2OUT (XT2) pins are multiplexed with the general-purpose I/O pins that reside on the DVCC supply domain. When the XT1 and XT2 oscillators are configured in crystal bypass mode, the XIN and XT2IN pins, respectively, can accept external clock input signals, and the XOUT and XT2OUT pins, respectively, can be configured as general-purpose I/O pins that are supplied by DVCC.

7 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using a serial interface. The F522x and F521x devices come with UART as the default BSL serial interface. Access to the device memory through the BSL is protected by a user-defined password. Because the F522x and F521x devices have split I/O power domains, it is possible to interface with the BSL from either the DVCC or DVIO supply domain.

Table 1 lists the device pins used for DVCC and DVIO supplied BSL interfaces. For more details, see the BSL description in MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers.

Table 1. DVCC and DVIO Supplied BSL Interfaces

BSL Function	DVCC Supplied BSL Interface	DVIO Supplied BSL Interface
External Reset	$\overline{\text{RSTDVCC}}$/SBWTDIO	$\overline{\text{RST}}$/NMI
Enable BSL	TEST/SBWTCK	BSLEN
Data Transmit	P1.1 (Timer_A UART)	P3.3/UCA0TXD (USCI_A0 UART)
Data Receive	P1.2 (Timer_A UART)	P3.4/UCA0RXD (USCI_A0 UART)
Device Power Supply	DVCC, AVCC	DVCC, AVCC
I/O Power Supply	DVIO	DVIO
Ground Supply	DVSS	DVSS

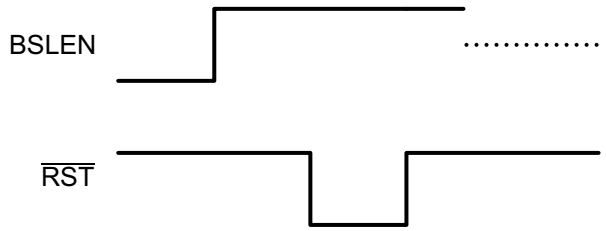
For single-supply systems (DVIO connected to DVCC) in which the DVCC supplied BSL interface is used, specific BSL entry and exit sequences are generated using the $\overline{\text{RSTDVCC}}$/SBWTDIO and TEST/SBWTCK pins. These are the standard RESET and TEST based BSL entry and exit sequences that apply to all non-USB F5xx and F6xx devices, and the standard TI supplied BSL tools can be used to access the device.

For split-supply I/O systems in which the DVIO supplied BSL interface is used, specific BSL entry and exit sequences should be generated using the $\overline{\text{RST}}$/NMI and BSLEN pins, and these sequences apply only to the DVIO supplied BSL interface.

NOTE: The default BSL loaded on these devices is the timer-based UART BSL in the DVCC domain. The USCI-based UART BSL in the DVIO domain must be loaded onto the device before being used. See the device user guide for more information. Also see the MSPBSL_CustomBSL430 Software download on the MSPBSL page for the DVIO-domain BSL image.

7.1 BSL Entry Sequence for DVIO Supplied BSL Interface

BSLEN is the BSL enable pin with internal pulldown resistor enabled and the BSL entry sequence involves toggling the $\overline{\text{RST}}$/NMI pin (high-low-high transition) with the BSLEN pin pulled high (see Figure 3).



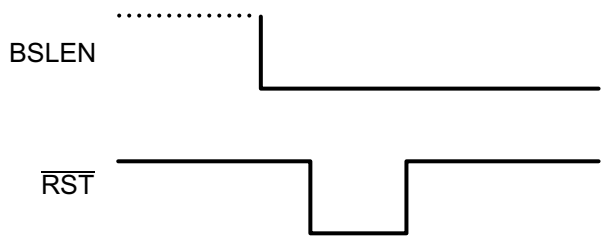
A The minimum timing for this sequence must be within the limits specified for the corresponding pins in the data sheet.

Figure 3. BSL Entry Sequence for DVIO Supplied BSL Interface

Note 2:The BSLEN pin need not be pulled high during the entire period when the device is in BSL mode. However, the BSLEN pin is required to be pulled high for a minimum period of time after the $\overline{\text{RST}}$/NMI pin goes low-high for proper BSL invoke. See the MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers data sheet for the timing specifications.

7.2 BSL Exit Sequence for DVIO Supplied BSL Interface

The BSL exit sequence of the DVIO supplied BSL interface involves toggling the $\overline{\text{RST}}$/NMI pin (high-low-high transition) with the BSLEN pin pulled low (see Figure 4).



A The minimum timing for this sequence must be within the limits specified for the corresponding pins in the data sheet.

Figure 4. BSL Exit Sequence for DVIO Supplied BSL Interface

For complete description of the BSL entry and exit sequences (for both DVCC and DVIO supplied BSL interfaces), features and its implementation, see the MSP430™ Flash Device Bootloader (BSL) User's Guide.

8 Debugger Connections

The F522x and F521x devices support both the standard four-wire JTAG interface and the two-wire Spy-Bi-Wire interface.

8.1 JTAG Standard Interface

The F522x and F521x support the standard JTAG interface. The four signals for receiving and sending JTAG signals are shared with Port J general-purpose I/Os and are powered by the DVCC supply domain. Table 2 lists the JTAG pin requirements. With the connections below, the JTAG can be used to interface with the MSP430 development tools and device programmers.

Table 2. Standard JTAG Interface Pins

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RSTDVCC}}$/SBWTDIO	IN	External reset
DVCC, AVCC		Device power supply
DVIO		I/O power supply
DVSS		Ground supply

For further details on interfacing to development tools and device programmers, see the MSP430™ Hardware Tool User's Guide.

8.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the F522x and F521x support the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with the MSP430 development tools and device programmers. The Spy-Bi-Wire signals are powered by the DVCC supply domain and Table 3 lists the interface pin requirements.

Table 3. Spy-Bi-Wire Interface Pins

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RSTDVCC}}$/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
DVCC, AVCC		Device power supply
DVIO		I/O power supply
DVSS		Ground supply

For further details on interfacing to development tools and device programmers, see the MSP430™ Hardware Tool User's Guide.

8.3 Debugging Without DVIO

It is safe and possible to have only DVCC and not DVIO connected to the device for the purpose of simple device debugging. However, DVIO pins and their related functions are not available in this mode. Additional effects include higher leakage current during debug; therefore, this option is suitable only for preliminary debugging of the device.

9 References

1. MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers
2. MSP430F5xx and MSP430F6xx Family User's Guide
3. MSP430™ Flash Device Bootloader (BSL) User's Guide
4. MSP430™ Hardware Tool User's Guide

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 30, 2012 to October 4, 2018 **Page**

- Updated titles and links to external documents, as needed 1
- Replaced "bootstrap loader" with "bootloader" throughout document 4
- Added the note that begins "The default BSL..." in Section 7, *Bootloader (BSL)* 5

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