Application Report
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TLV320AIC32x4 Power Supply Sequencing

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ABSTRACT

The TLV320AIC32x4 is capable of multiple power supply configurations. Power can be applied externally to support multiple voltage levels as well as internal generation of the analog and digital supply. This document discusses proper supply sequencing for these configurations.

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1 Introduction

This document is divided into two parts: external supply configurations and internal supply configurations. The application report SLAA404 and the relevant product data sheet provide detailed information on power supply configurations. The TLV320AIC32x4 power management architecture is shown in Figure 1 as a reference.

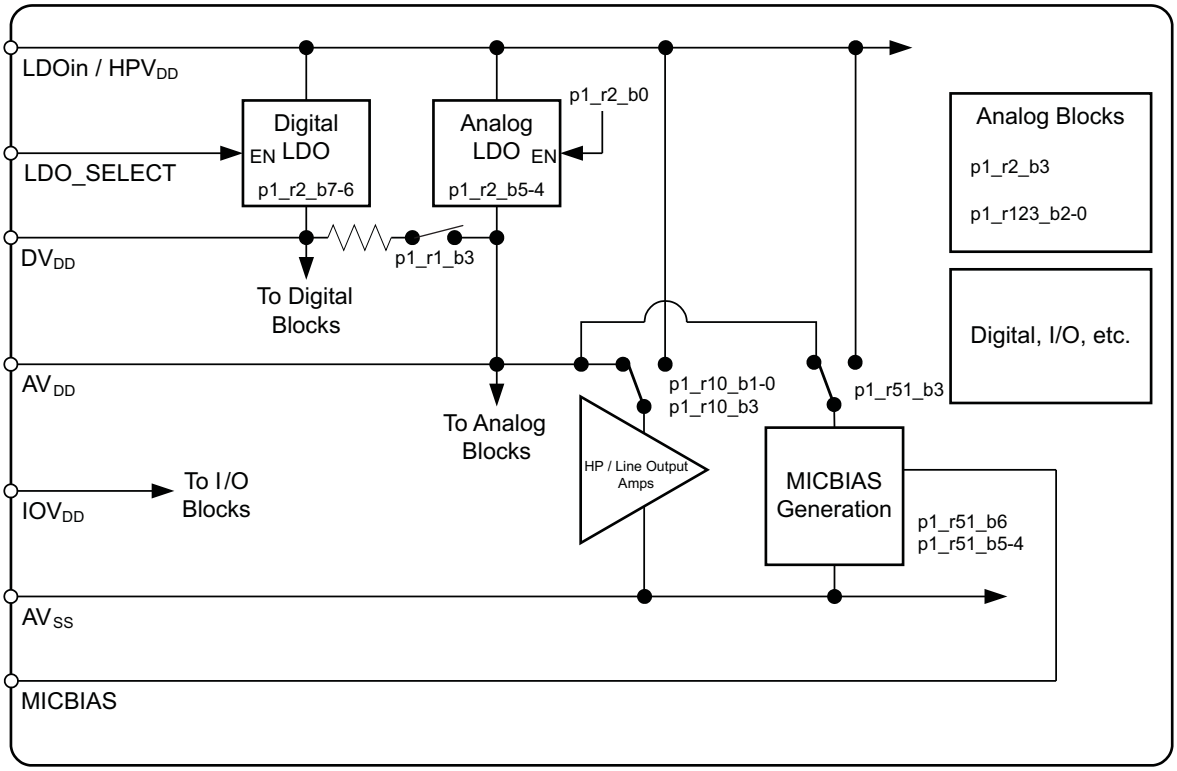

Figure 1. TLV320AIC32x4 Power Management Architecture

2 External DV_{DD} and AV_{DD} Power Supply Sequence

The recommended power sequence for this configuration is to provide all supplies simultaneously. A typical configuration in such a case is to use a single 1.8-V supply for IOV_{DD}, DV_{DD}, LDOin, and AV_{DD}.

Another alternative is to separate analog and digital supplies. This is useful to improve the efficiency of the digital rails by using a dc/dc converter, while keeping the AV_{DD} supply clean by using a low-dropout regulator (LDO). This LDO can be external or internal.

The LDOin supply can be sourced by an external supply of 1.9 V to 3.6 V to allow a higher signal swing at the headphone and line-out amplifiers, as well as to provide a wider range of MICBIAS supply options and output common-mode voltage. In the case where a 1.8-V rail is sufficient for output swing, LDOin must be tied to AV_{DD}.

Figure 2 shows a timing diagram for the case where all supplies are provided separately. In such a case, the depicted sequence must be used. The dashed lines marked in blue color represent an internally supplied voltage.

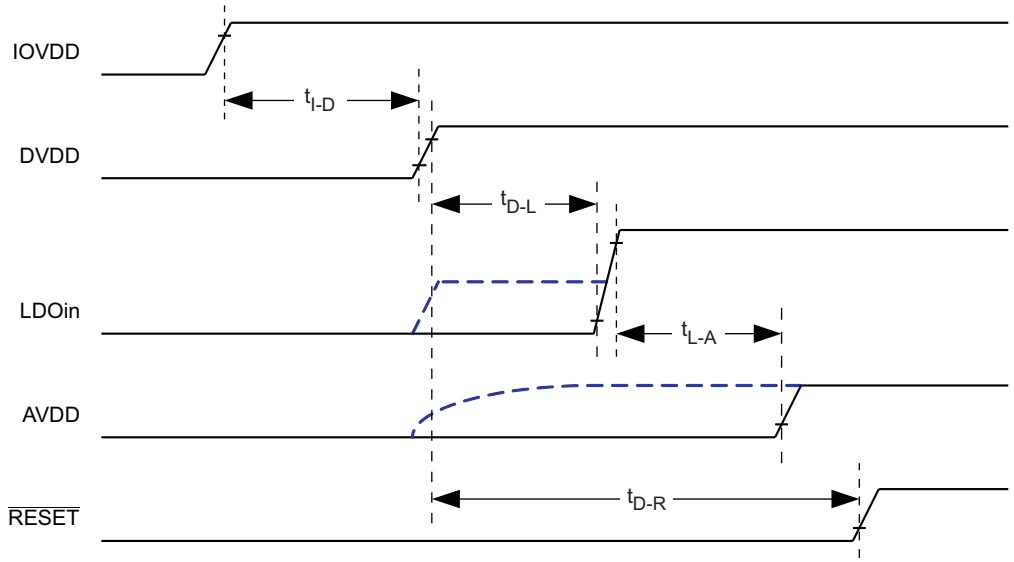

Figure 2. DV_{DD} and AV_{DD} Externally Provided

IOV_{DD} must be provided first. Because, by default, DV_{DD} is weakly connected to AV_{DD} by a 10-kΩ resistor, AV_{DD} ramps up to the DV_{DD} voltage once DV_{DD} is provided at approximately 5 × 10 kΩ × C_{AVDD}, where C_{AVDD} is the A_{VDD} decoupling capacitor. For C_{AVDD} = 1 µF, the charging time is approximately 50 ms. Parameter t_{D-L} allows AV_{DD} to be stable before HPVDD is provided, which prevents power-on pop on the headphone amplifiers. Immediately after DV_{DD} is provided, the LDOin supply ramps to ~1.5 V. To prevent high currents from DVDD to LDOin, the LDOin supply cannot be externally driven low by the external power source. This means that the external power source must be either high impedance or have a weak pulldown before being enabled. After $\overline{\text{RESET}}$ is released (or a software reset is performed), no register writes must be performed within 1 ms.

Table 1. Power Supply Timing Parameters

PARAMETER	MIN	TYP	MAX	COMMENTS
t_{I-D}	0	0		Time between IOVDD is provided and DV_{DD} is provided.
t_{D-L}	5×10k×C_{AVDD}	5×10k×C_{AVDD}		Time between DV_{DD} is provided and LDOin is provided. AV_{DD} must be internally present before LDOin to prevent pop at headphone outputs.
t_{L-A}	0	0		Time between LDOin is provided and AV_{DD} is externally provided.
t_{D-R}	10 ns	10 ns		Time between DV_{DD} (and IOVDD) is provided and reset can be released.

AV_{DD} can also be externally supplied at the same time as DV_{DD}. This is shown in Figure 3. The dashed line marked in blue color represents an internally supplied voltage.

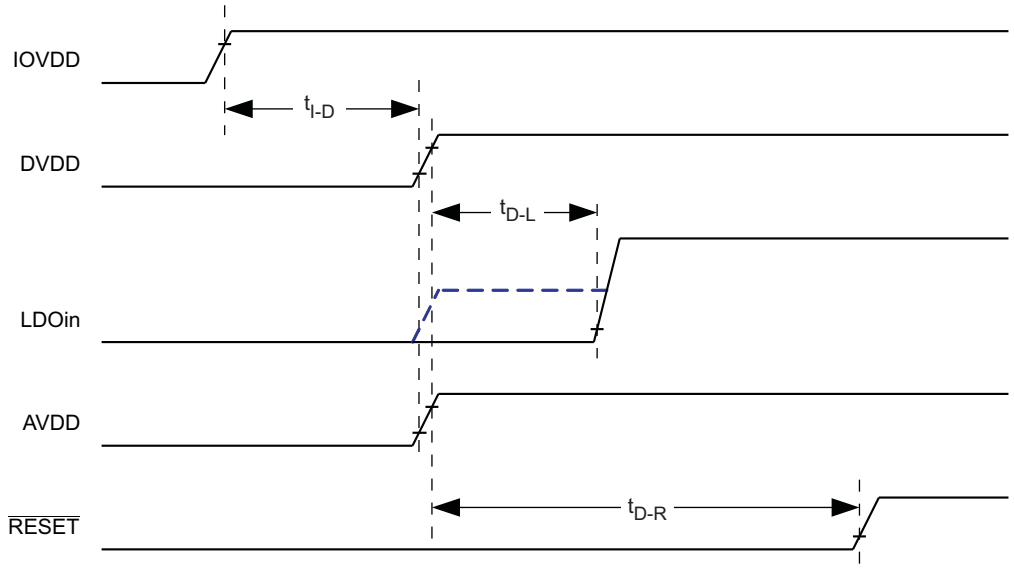

Figure 3. DV_{DD} and AV_{DD} Externally Provided, AV_{DD} Together With DV_{DD}

To prevent high currents from DV_{DD} to LDOin, the LDOin supply cannot be externally driven low by the external power source. This means that the external power source must be either high impedance or have a weak pulldown before being enabled.

After $\overline{\text{RESET}}$ is released (or a software reset is performed), no register writes must be performed within 1 ms.

Table 2. Power Supply Timing Parameters

PARAMETER	MIN	TYP	MAX	COMMENTS
t_{I-D}	0	0		Time between IOVDD is provided and DV_{DD} (and AV_{DD}) is provided.
t_{D-L}	0	0		Time between DV_{DD} (and AV_{DD}) is provided and LDOin is provided.
t_{D-R}	10 ns	10 ns		Time between DV_{DD} (and IOVDD) is provided and reset can be released.

3 Internal DLDO and ALDO Power Supply Sequence

Generating DV_{DD} and AV_{DD} internally is a common configuration for systems where a single 3.3-V supply is used. The DLDO is enabled by tying the LDO_SELECT pin to the IOVDD supply. As soon as IOVDD and LDOin are provided, DV_{DD} ramps to a nominal 1.72 V. At the same time, the AV_{DD} pin ramps up slower (5 × 10 kΩ × C_{AVDD}) which might result in a pop in the headphone output amplifiers if C_{AVDD} is initially discharged. This pop can be avoided by adding a Schottky diode between DV_{DD} and AV_{DD} pins as shown in Figure 4. Note that, in this configuration, ALDO mode must be chosen such that AV_{DD} voltage is higher than or equal to DV_{DD} voltage. For example, ALDO can be configured as 1.77 V and DLDO as 1.77 V, or ALDO as 1.77 V and DLDO as 1.72 V.

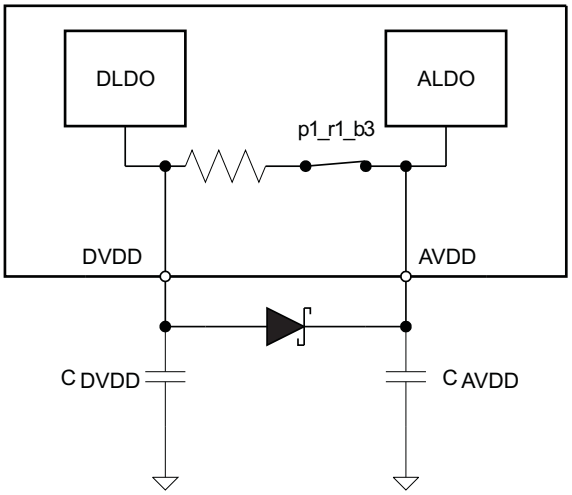

Figure 4. Recommended Circuit to Avoid Headphone Pop

If the internal headphone amplifiers are connected to an external amplifier with mute or shutdown capabilities, it is unnecessary to add a diode. The purpose of this diode is to force the AV_{DD} pin to ramp close to the DV_{DD} voltage at the same time and rate as LDOin is provided.

Figure 5 shows the timing diagram for the case where DV_{DD} and AV_{DD} are supplied by the internal LDOs and an external Schottky diode is placed between DV_{DD} and AV_{DD}. The dashed line marked in blue color illustrates the voltage supplied through the external diode. The lines marked in red color illustrate a voltage generated by the internal LDOs.

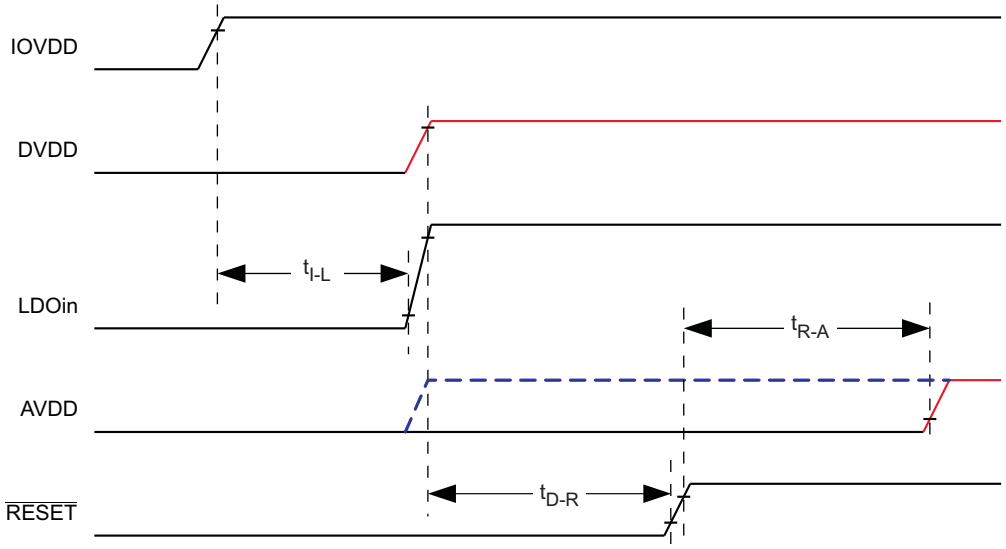

Figure 5. DV_{DD} and AV_{DD} Generated by Internal LDO

As previously mentioned, if the internal headphone amplifiers are connected to an external amplifier with mute or shutdown capabilities, an external diode is not required. For such a case, AV_{DD} ramps to DV_{DD} in approximately 5 × 10 kΩ × C_{AVDD}.

Table 3. Power Supply Timing Parameters

PARAMETER	MIN	TYP	MAX	COMMENTS
t_{I-D}	0	0		Time between IOVDD is provided and LDOin is provided.
t_{D-R}	10 ns	10 ns		Time between DVDD (and IOVDD) is provided and reset can be released.
t_{R-A}	1 ms	1 ms		Time between $\overline{\text{RESET}}$ is released and ALDO is powered. No registers must be written for 1 ms after a reset is performed (hardware or software).

4 References

1. *Design and Configuration Guide for the TLV320AI3204 and TLV320AIC3254 Audio Codecs* application report (SLAA404)
2. *TLV320AIC3254, Ultra Low Power Stereo Audio Codec With Embedded miniDSP* data sheet (SLAS549)
3. *TLV320AIC3204, Ultra Low Power. Stereo Audio Codec* data sheet (SLOS602)

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