Application Report
SLAA468B –October 2010–Revised September 2014

TLV320AIC31xx and TLV320DAC31xx Power Consumption Characterization

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ABSTRACT

One of the main properties of the TLV320AIC31xx and TLV320DAC31xx audio converter family is low power consumption. Power consumption can be tuned to minimize power consumption and maximize the performance. This application report provides a detailed description with scripts for setting up the TLV320AIC31xx and TLV320DAC31xx devices for minimum power consumption. The document also compares different-use cases in their corresponding power consumption and performance. Throughout this document, TLV320AIC31xx/DAC31xx is used as an abbreviation for TLV320AIC31xx and TLV320DAC31xx.

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1 Introduction

The TLV320AIC31xx/DAC31xx is a low-power data converter family with devices that include a high-performance audio codec with 16-bit stereo playback and monaural record functionality, a fully programmable mini DSP for digital audio processing, and a built-in PLL to provide a high-speed clock to the digital signal processing blocks. Register-based architecture is used in these data converters and eases integration with a microprocessor-based system through standard serial interface buses.

This converter family can be tuned to minimize the power consumption and increase the performance. This can be achieved by choosing the right processing block for the required application and powering down the unused blocks. This allows power optimization without any disconnecting external supplies. That is done by simply writing to the control registers. Also, the TLV320AIC31xx/DAC31xx devices have a software-capability to power down without disconnecting any external power supply.

The following application report provides the characterization of power consumption of the TLV320AIC31xx/DAC31xx converters for stereo playback via headphones, stereo playback via headphones and speakers, mono record, mono record plus stereo playback via headphones, and mono record plus stereo playback via headphones and speakers. Scripts of each application are provided and the register setting for power optimization for different blocks are described.

2 General Setup Description

Based on the available master clock, the chosen AOSR/DOSR, and the targeted sampling rate, the clock divider values NADC/MADC and NDAC/MDAC can be determined. If necessary, the internal PLL can be added for a large degree of flexibility. The PLL can be set by choosing value for P, R, J, and D coefficients.

For lower power consumption, it is desirable to power down the PLL. However, not using the PLL requires the right settings for the NDAC and MDAC coefficients to obtain a proper operation of the converter. These coefficients can be chosen independently in the range of 1 to 128. In general, the NDAC coefficient must be as large as possible, as long as MADC × AOSR / 32 is greater than or equal to RC. RC is defined as the Resource Classes of each processing block that are provided in the detailed data sheet.

In the following applications, the converter receives a master clock of 11.2896 MHz. In most of the processing blocks, the PLL is turned off. The NDAC and MDAC are set to 1 and 2, respectively. In case the preceding condition is not met for a specific processing block, the PLL is required. For lower power consumption with the PLL on, the coefficients NDAC and MDAC are set to 2 and 8, respectively. A value of 4 for both of MDAC and NDAC also can be used. The PLL settings are given as follows: P = 1, R = 1, J = 8, and D = 0.

The processing blocks of the mini DSP have direct impact on power consumption and performance of the TLV320AIC31xx/DAC31xx converters. Thus, choosing the right processing block in both record and playback is important. The processing blocks configuration can be done using registers 60 and 61 in page 0 for both playback and record, respectively.

The DAC and the ADC needs a proper configuration for lower power consumption. In playback only, the ADC is not needed; therefore it must be powered down. The same thing is required with the DAC in record mode. The class-D driver and the left/right speaker need to be powered down during record, playback via headphones, and record plus playback via headphones modes because they are not used.

The TLV320AIC31xx/DAC31xx devices have the capability of being turned off using register settings without turning off or disconnecting the device from the power supplies. Powering down the device can be done using register 46 on page 01 and enabling the device power-down option on D7. The following two instructions turn down the device: (1) selecting page 0 "w 30 00 01", and (2) device software power down enabling "w 30 2e 80".

2.1 Test Setup

All tests are done on a TLV320AIC3111EVM (Rev A), the super set device for the TLV320AIC31xx/DAC31xx audio converter family. The data found in this application note applies to the entire AIC31xx/DAC31xx converter family as long as that device has the functionality of the application of interest (that is, the Mono Record section only applies to the devices with ADCs). The tests are done by cutting the wire loops at W10, 11, 12, 13, and 14 and placing a multimeter in series with each rail to measure current. For all stereo playback testing, the device is first configured and programmed and then the DAC modulator is excited by playing a few seconds of sound after which, the sound is stopped and the current measurement is taken. For all tests that include the headphone amplifier, a 16-Ω resistor in series with a 100-µH inductor is used as a load for each channel. For all tests that include the class D speaker output, an 8-Ω resistor in series with a 33-µH inductor is used as a load for each channel. The sampling frequency for all cases is 44.1 kHz.

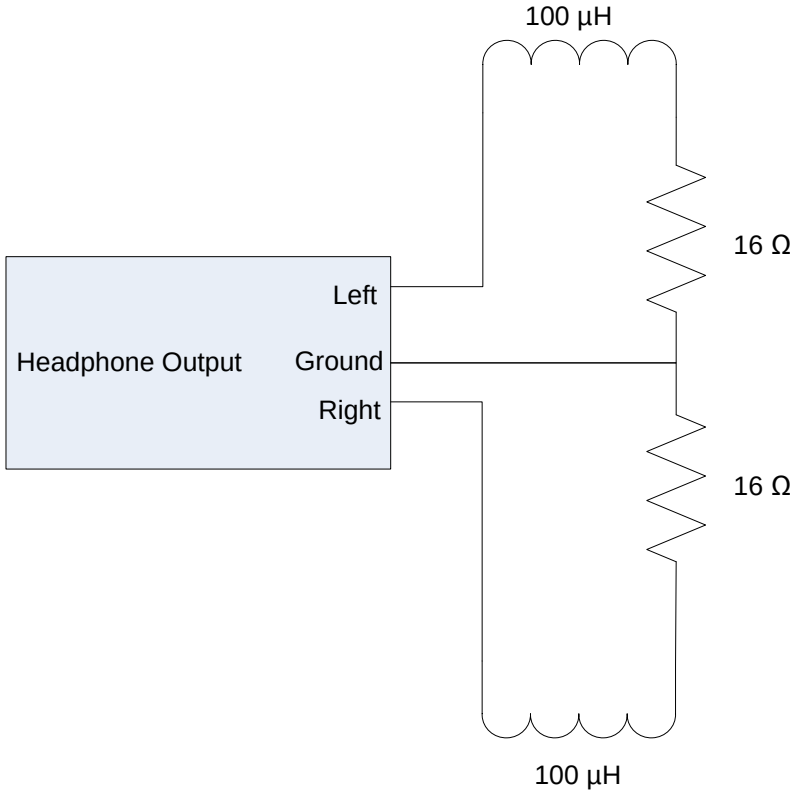

Figure 1. Headphone Output

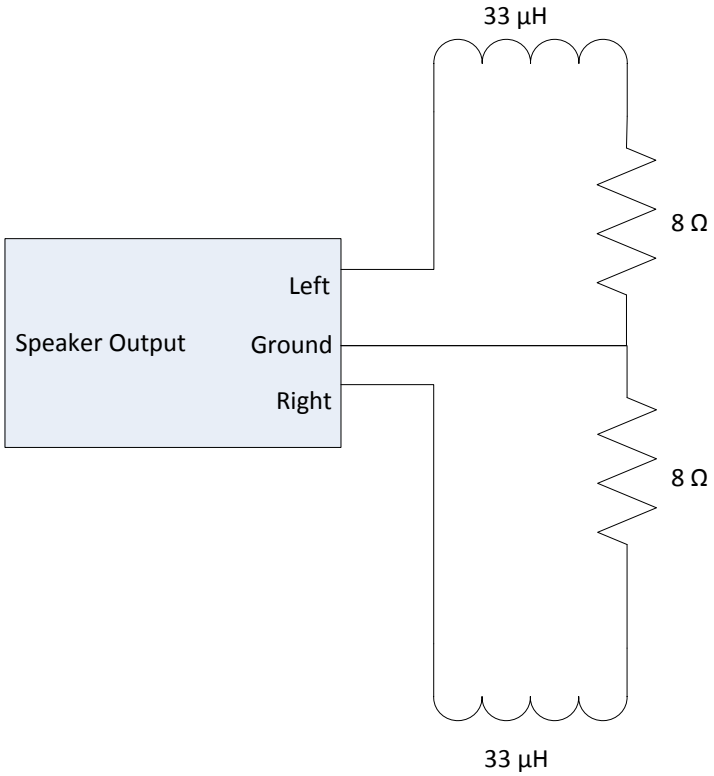

Figure 2. Speaker Output

2.2 Stereo Playback via Headphone

The stereo playback via headphone power consumptions of the converter are provided in the following tables. A 16-Ω resistor in series with a 100-µH inductor is connected to the headphone output for these measurements. Different processing blocks are used during the measurements. A script is provided at the end of this section. For devices with a mono DAC there is approximately a 6.8-mW power saving for headphone applications. The savings come from powering only a single DAC (gives 0.8 mW power savings) and having only a single headphone amplifier powered (6.0 mW power savings).

Table 1. Power Consumption for Stereo Playback via Headphones With PRB-P7 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.50	—	N/A
Power (mW)	8.514	0	0	11.418	4.500	—	24.432

Table 2. Power Consumption for Stereo Playback via Headphones With PRB-P1 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.90	—	N/A
Power (mW)	8.514	0	0	11.418	5.220	—	25.152

Table 3. Power Consumption for Stereo Playback via Headphones With PRB-P2 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.34	—	N/A
Power (mW)	8.514	0	0	11.418	4.212	—	24.144

Table 4. Power Consumption for Stereo Playback via Headphones With PRB-P3 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.36	—	N/A
Power (mW)	8.514	0	0	11.418	4.248	—	24.180

Table 5. Power Consumption for Stereo Playback via Headphones With PRB-P8 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	3.00	—	N/A
Power (mW)	8.514	0	0	11.418	5.400	—	25.332

Table 6. Power Consumption for Stereo Playback via Headphones With PRB-P9 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (Volt)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.32	—	N/A
Power (mW)	8.514	0	0	11.418	4.176	—	24.108

Table 7. Power Consumption for Stereo Playback via Headphones With PRB-P10 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.24	—	N/A
Power (mW)	8.514	0	0	11.418	4.032	—	23.964

Table 8. Power Consumption for Stereo Playback via Headphones With PRB-P11 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.75	—	N/A
Power (mW)	8.514	0	0	11.418	4.950	—	24.882

Table 9. Power Consumption for Stereo Playback via Headphones With PRB-P23 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.88	—	N/A
Power (mW)	8.514	0	0	11.418	5.184	—	25.116

Table 10. Power Consumption for Stereo Playback via Headphones With PRB-P24 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.32	—	N/A
Power (mW)	8.514	0	0	11.418	4.176	—	24.108

Table 11. Power Consumption for Stereo Playback via Headphones With PRB-P25 Processing Block

STEREO PLAYBACK via HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.58	0	0	3.46	2.41	—	N/A
Power (mW)	8.514	0	0	11.418	4.338	—	24.270

```
######## SCRIPT FOR STEREO PLAYBACK VIA HEAD PHONES
# Software Reset
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Clock and Interface Settings
# The codec receives: MCLK = 11.2896 MHz,
# BLCK = 2.8224 MHz, WCLK = 44.1 kHz
# If PLL is used, set NDAC=1, MDAC=2
# If PLL is not used set NDAC=2 MDAC=8
# Select Page 0
w 30 00 00
# PLL_clkin = MCLK, codec_clkin = PLL_CLK,
# PLL on, P=1, R=1, J=8, D=0000
# w 30 04 03 91 08 00 00
# Comment this line to disable the PLL
# NDAC =1, MDAC = 2, dividers powered on
w 30 0b 81 82
# DOSR = 128
w 30 0D 00 80
# NADC = 1, MADC = 2, dividers powered on
w 30 12 81 82
# AOSR = 128
w 30 14 80
#############################################################################
# Processing Blocks Configuration
# Select Page 0
w 30 00 00
# DAC Processing PRB_P7, change the processor as needed
w 30 3c 07
# Configure DAC Channel
# Select Page 01
w 30 00 01
# DACs routed to Mixer Amplifiers
w 30 23 44 # Switch to Page 0
w 30 00 00
# Powerup DACs
w 30 3f D4
# Unmute DACs, 0dB
w 30 40 00 00 00
#############################################################################
# Configure ADC Channel
# Switch to Page 0
w 30 00 00
# POWERDOWN ADC channel
w 30 51 00
```

```
########################################################################
# Configure L/R Head Phone Output
# Select Page 1
w 30 00 01
# De-pop, Power on = 1.22s, Step time = 3.9 ms
w 30 21 4e
# Route HPL and HPR Analog Volume Control, 0dB
w 30 24 80 80
# HPL and HPR Power up, current limit, CM = 1.65V
w 30 1f d4
# HPL and HPR unmute and gain 0db
w 30 28 06 06
########################################################################
# Configure L/R Speakers Output
# Power Down Class-D drivers for less power
w 30 20 06
######################### END OF SCRIPT ##########################
```

2.3 Stereo Playback via Headphones and Speakers

The following section provides the power consumption of the converter in stereo playback via headphones and speakers at the same time. An 8-Ω resistor in series with a 33-µH inductor is connected to the speaker output and a 16-Ω resistor in series with a 100-µH inductor is connected to the headphone output for these measurements. A detailed script for this use case is provided at the end of this section.

The ADC is required only for record; thus, it is turned off.

Table 12. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P7 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.50	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.500	—	74.748

Table 13. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P1 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.95	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	5.310	—	75.558

Table 14. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P2 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.39	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.302	—	74.550

Table 15. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P3 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.33	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.194	—	74.442

Table 16. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P8 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.93	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	5.274	—	75.522

Table 17. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P9 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.70	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.860	—	75.108

Table 18. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P10 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.29	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.122	—	74.370

Table 19. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P11 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.74	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.932	—	75.180

Table 20. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P23 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.89	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	5.202	—	75.450

Table 21. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P24 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.38	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.284	—	74.532

Table 22. Power Consumption for Stereo Playback via Headphones and Speaker With PRB-P25 Processing Block

S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.95	3.69	5.81	7.11	2.37	—	N/A
Power (mW)	9.735	14.391	22.659	23.463	4.266	—	74.514

```
######## SCRIPT FOR STEREO PLAYBACK VIA HEAD PHONES AND SPEAKERS
# Software Reset
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Clock and Interface Settings
# The codec receives: MCLK = 11.2896 MHz,
# BLCK = 2.8224 MHz, WCLK = 44.1 kHz
# If PLL is used, set NDAC=1, MDAC=2
# If PLL is not used set NDAC=2 MDAC=8
# Select Page 0
w 30 00 00
# PLL_clkin = MCLK, codec_clkin = PLL_CLK,
# PLL on, P=1, R=1, J=8, D=0000
# w 30 04 03 91 08 00 00
# Comment this line to disable the PLL
# NDAC =1, MDAC = 2, dividers powered on
w 30 0b 81 82
# DOSR = 128
w 30 0D 00 80
# NADC = 1, MADC = 2, dividers powered on
w 30 12 81 82
# AOSR = 128
w 30 14 80
#############################################################################
# Processing Blocks Configuration
# Select Page 0
w 30 00 00
# PRB_P7, Processing blocks selection
w 30 3c 07
#############################################################################
# Configure ADC Channel
# Select Page 0
w 30 00 00
# POWERDOWN ADC channel
w 30 51 00
#############################################################################
# Configure DAC Channel
# Switch to Page 1
w 30 00 01
# DACs routed to Mixer Amplifiers 44
w 30 23 44
# Switch to Page 0
w 30 00 00 # Powerup DACs
w 30 3f D4
# Unmute DACs, 0dB
w 30 40 00 00 00
#############################################################################
# Configure HP Output
# Switch to Page 1
w 30 00 01
# De-pop, Power on = 1.22s, Step time = 3.9 ms
w 30 21 4e
# Route HPL and HPR Analog Volume Control, 0dB
w 30 24 80 80
# HPL and HPR Power up, current limit, CM = 1.65V
w 30 1f d4
# HPL and HPR unmute and gain 0db
w 30 28 06 06
#############################################################################
# Configure SPK Output
# Configure Class-D
w 30 26 80 80
# 24dB gain
w 30 2a 04 04
```

```
# Unmute Class-D Left
w 30 2a 1c
# Unmute Class-D Right
w 30 2b 1c
# Power up Class-D drivers
w 30 20 C6
######################## END OF SCRIPT ########################
```

2.4 Mono Record

Mono record use case is considered in this section. All the unused blocks of the converter such as DAC, class-D driver, and the speakers are powered down. The power consumption is measured both with and without using PLL.

Table 23. Power Consumption for Record With PRB-R4 Processing Block

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.34	0	0	0	1.19	—	N/A
Power (mW)	7.722	0	0	0	2.142	—	9.864

Table 24. Power Consumption for Record With PRB-R5 Processing Block

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.34	0	0	0	1.31	—	N/A
Power (mW)	7.722	0	0	0	2.358	—	10.080

Table 25. Power Consumption for Record With PRB-R6 Processing Block

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.34	0	0	0	1.30	—	N/A
Power (mW)	7.722	0	0	0	2.340	—	10.062

Table 26. Power Consumption for Record With PRB-R4 Processing Block and With PLL Turned On

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.44	0	0	1.15	2.14	—	N/A
Power (mW)	8.052	0	0	3.795	3.852	—	15.699

Table 27. Power Consumption for Record With PRB-R5 Processing Block and With PLL Turned On

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	2.44	0	0	1.15	2.26	—	N/A
Power (mW)	8.052	0	0	3.795	4.068	—	15.915

Table 28. Power Consumption for Record With PRB-R6 Processing Block and With PLL Turned On

MONO RECORD	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Currents (mA)	2.44	0	0	1.15	2.25	—	N/A
Power (mW)	8.052	0	0	3.795	4.050	—	15.897

```
################ SCRIPT FOR MONO RECORD
# Software Reset
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Clock and Interface Settings
# The codec receives: MCLK = 11.2896 MHz,
# BLCK = 2.8224 MHz, WCLK = 44.1 kHz
# If PLL is used, set NDAC=1, MDAC=2
# If PLL is not used set NDAC=2 MDAC=8
# Select Page 0
w 30 00 00
# PLL_clkin = MCLK, codec_clkin = PLL_CLK,
# PLL on, P=1, R=1, J=8, D=0000
# w 30 04 03 91 08 00 00
# Comment this line to disable the PLL
# NDAC =1, MDAC = 2, dividers powered on
w 30 0b 81 82
# DOSR = 128
w 30 0D 00 80
# NADC = 1, MADC = 2, dividers powered on
w 30 12 81 82
# AOSR = 128
w 30 14 80
###########################################################################
# Processing Blocks Configuration
# Select Page 0
w 30 00 00
# PRB_R04, Processing blocks selection
w 30 3d 04
###########################################################################
# Configure ADC Channel
# Switch to Page 1
w 30 00 01
# Programmed MICBIAS always on, 2.5V
w 30 2E 0A
# MICPGA P = MIC1LP 20kohm
w 30 30 80
# MICPGA M – CM 20kohm
w 30 31 80
# Switch to Page 0
w 30 00 00
# POWERUP ADC channel, UNMUTE
w 30 51 80 00
d 100
w 30 00 01
# MIC input set up
w 30 30 c0
w 30 31 c0
###########################################################################
# Configure DAC Channel
# Switch to Page 1
w 30 00 01
# DACs routed to Mixer Amplifiers 44h
# w 30 23 44
# Switch to Page 0
# w 30 00 00
# Power Down DACs
# w 30 3f 00
# DAC is powered down by default
###########################################################################
# Configure HP Output
# Switch to Page 1
w 30 00 01
# De-pop, Power on = 1.22s, Step time = 3.9 ms
```

```
w 30 21 4e
# Route HPL and HPR Analog Volume Control, 0dB
w 30 24 80 80
# HPL and HPR power down, current limit, CM = 1.65V
w 30 1f 04
# HPL and HPR unmute and gain 0db (02 OR 00)
w 30 28 02 02
##############################################################################
# Configure SPK Output
# Power down Class-D drivers
w 30 20 06
######################### END OF SCRIPT ########################
```

2.5 Mono Record Plus Stereo Playback via Headphone

Mono record plus stereo playback via headphone is considered in this section. A 16-Ω resistor in series with a 100-µH inductor is connected to the headphone output for these measurements. The class-D drivers and the left and right speakers are not needed in this use case. Different processing blocks are used and power consumption of each of them is given as follows:

Table 29. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P7 and PRB-R4 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	3.53	—	N/A
Power (mW)	15.543	0	0	11.385	6.354	—	33.282

Table 30. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P7 and PRB-R5 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	3.64	—	N/A
Power (mW)	15.543	0	0	11.385	6.552	—	33.480

Table 31. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P1 and PRB-R4 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	4.28	—	N/A
Power (mW)	15.543	0	0	11.385	7.704	—	34.632

Table 32. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P1 and PRB-R5 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	4.39	—	N/A
Power (mW)	15.543	0	0	11.385	7.902	—	34.830

Table 33. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P9 and PRB-R4 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	3.84	—	N/A
Power (mW)	15.543	0	0	11.385	6.912	—	33.840

Table 34. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P9 and PRB-R5 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	3.95	—	N/A
Power (mW)	15.543	0	0	11.385	7.110	—	34.038

Table 35. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P11 and PRB-R4 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	3.97	—	N/A
Power (mW)	15.543	0	0	11.385	7.146	—	34.074

Table 36. Power Consumption for Record Plus Stereo Playback via Headphones With PRB-P11 and PRB-R5 Processing Blocks

M RECORD +S PLAYBACK VIA HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	4.71	0	0	3.45	4.09	—	N/A
Power (mW)	15.543	0	0	11.385	7.362	—	34.290

```
######### SCRIPT FOR MONO RECORD PLUS STEREO PLAYBACK via HEADPHONES
#######
# Software Reset
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Clock and Interface Settings
# The codec receives: MCLK = 11.2896 MHz,
# BLCK = 2.8224 MHz, WCLK = 44.1 kHz
# If PLL is used, set NDAC=1, MDAC=2
# If PLL is not used set NDAC=2 MDAC=8
# Select Page 00
w 30 00 00
# PLL_clkin = MCLK, codec_clkin = PLL_CLK,
# PLL on, P=1, R=1, J=8, D=0000
# w 30 04 03 91 08 00 00
# Comment this line to disable the PLL
# NDAC =1, MDAC = 2, dividers powered on
w 30 0b 81 82
# DOSR = 128
w 30 0D 00 80
# NADC = 1, MADC = 2, dividers powered on
w 30 12 81 82
# AOSR = 128
w 30 14 80
#############################################################################
# Processing Blocks Configuration
# Select Page 0
w 30 00 00
# PRB_P7 PRB-R04, Processing blocks selection
w 30 3c 07 04
#############################################################################
# Configure ADC Channel
# Switch to Page 1
w 30 00 01
# Programmed MICBIAS always on, 2.5V
w 30 2E 0A
# MICPGA P = MIC1LP 20kohm
w 30 30 80
# MICPGA M – CM 20kohm
w 30 31 80
# Switch to Page 0
w 30 00 00
# POWERUP ADC channel, UNMUTE
w 30 51 80 00
d 100
```

```
w 30 00 01
# MIC input set up
w 30 30 c0
w 30 31 c0
########################################################################
# Configure DAC Channel
# Switch to Page 1
w 30 00 01
# DACs routed to Mixer Amplifiers
w 30 23 44
# Switch to Page 0
w 30 00 00
# Power up DACs
w 30 3f D4
# Unmute DACs, 0dB
w 30 40 00 00 00
########################################################################
# Configure HP Output
# Switch to Page 1
w 30 00 01
# De-pop, Power on = 1.22s, Step time = 3.9 ms
w 30 21 4e
# Route HPL and HPR Analog Volume Control, 0dB
w 30 24 80 80
# HPL and HPR power down, current limit, CM = 1.65V
w 30 1f d4
# HPL and HPR unmute and gain 0db
w 30 28 06 06
########################################################################
# Configure SPK Output
# Power down Class-D drivers
w 30 20 06
########################################################################
# Configure the looping ADC with DAC
# Loop ADC-DAC
w 30 00 00
w 30 1d 10
######################### END OF SCRIPT ##########################
```

2.6 Mono Record Plus Stereo Playback via Headphone and Speakers

In this section, Mono record plus stereo playback via both headphone and speakers is considered. An 8-Ω resistor in series with a 33-µH inductor is connected to the speaker output and 16-Ω resistor in series with a 100-µH inductor is connected to the headphone output for these measurements. The power consumption of the converter in this use case is provided for different processing blocks.

Table 37. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P7 and PRB-R4 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	1.71	2.01	7.11	3.53	—	N/A
Power (mW)	16.896	6.669	7.839	23.463	6.354	—	61.221

Table 38. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P7 and PRB-R5 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	1.71	2.01	7.11	3.64	—	N/A
Power (mW)	16.896	6.669	7.839	23.463	6.552	—	61.419

Table 39. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P1 and PRB-R4 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	1.71	2.01	7.11	4.27	—	N/A
Power (mW)	16.896	6.669	7.839	23.463	7.686	—	62.553

Table 40. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P1 and PRB-R5 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	1.71	2.01	7.11	4.39	—	N/A
Power (mW)	16.896	6.669	7.839	23.463	7.902	—	62.769

Table 41. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P9 and PRB-R4 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	3.71	5.82	7.11	3.84	—	N/A
Power (mW)	16.896	14.469	22.698	23.463	6.912	—	84.438

Table 42. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P9 and PRB-R5 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	3.71	5.82	7.11	3.93	—	N/A
Power (mW)	16.896	14.469	22.698	23.463	7.074	—	84.600

Table 43. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P11 and PRB-R4 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	3.71	5.82	7.11	3.95	—	N/A
Power (mW)	16.896	14.469	22.698	23.463	7.110	—	84.636

Table 44. Power Consumption for Record Plus Stereo Playback via Headphones and Speakers With PRB-P11 and PRB-R5 Processing Blocks

MR+S PLAYBACK via SPK/HP	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (mA)	5.12	3.71	5.82	7.11	4.06	—	N/A
Power (mW)	16.896	14.469	22.698	23.463	7.308	—	84.834

```
######### SCRIPT FOR MONO RECORD STEREO PLAYBACK via HEADPHONES AND SPEAKERS #######
# Software Reset
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Clock and Interface Settings
# The codec receives: MCLK = 11.2896 MHz,
# BLCK = 2.8224 MHz, WCLK = 44.1 kHz
# If PLL is used, set NDAC=1, MDAC=2
# If PLL is not used set NDAC=2 MDAC=8
# Select Page 00
w 30 00 00
# PLL_clkin = MCLK, codec_clkin = PLL_CLK,
# PLL on, P=1, R=1, J=8, D=0000
# w 30 04 03 91 08 00 00
# Comment this line to disable the PLL
# NDAC =1, MDAC = 2, dividers powered on
w 30 0b 81 82
# DOSR = 128
w 30 0D 00 80
# NADC = 1, MADC = 2, dividers powered on
w 30 12 81 82
# AOSR = 128
w 30 14 80
#############################################################################
# Processing Blocks Configuration
# Select Page 0
w 30 00 00
# PRB_P7 PRB-R04, Processing blocks selection
w 30 3c 07 04
#############################################################################
# Configure ADC Channel
# Switch to Page 1
w 30 00 01
# Programmed MICBIAS always on, 2.5V
w 30 2E 0A
# MICPGA P = MIC1LP 20kohm
w 30 30 80
# MICPGA M – CM 20kohm
w 30 31 80
# Switch to Page 0
w 30 00 00
# POWERUP ADC channel, UNMUTE
w 30 51 80 00
d 100
w 30 00 01
```

```
# MIC input set up
w 30 30 c0
w 30 31 c0
########################################################################
# Configure DAC Channel
# Switch to Page 1
w 30 00 01
# DACs routed to Mixer Amplifiers 44
w 30 23 44
# Switch to Page 0
w 30 00 00
# Power up DACs
w 30 3f D4
# Unmute DACs, 0dB
w 30 40 00 00 00
########################################################################
# Configure HP Output
# Switch to Page 1
w 30 00 01
# De-pop, Power on = 1.22s, Step time = 3.9 ms
w 30 21 4e
# Route HPL and HPR Analog Volume Control, 0dB
w 30 24 80 80
# HPL and HPR power down, current limit, CM = 1.65V
w 30 1f d4
# HPL and HPR unmute and gain 0db
w 30 28 06 06
# Configure SPK Output
# Configure Class-D
w 30 26 80 80
# 24dB gain
w 30 2a 04 04
# Unmute Class-D Left
w 30 2a 1c
# Unmute Class-D Right
w 30 2b 1c
# Power up Class-D drivers
w 30 20 C6
# Configure the loop back of DAC with ADC
# Loop Back
w 30 00 00
w 30 1d 10
######################### END OF SCRIPT ##########################
```

2.7 Power-Down Mode

The TLV320AIC31xx/DAC31xx devices can be turned off without disconnecting any of their power supplies. Table 45 provides measurements of power consumption in this mode. Note that the range of power measurements is in microwatts (µW). The following two instructions power down the codec: (1) selecting page 0 "w 30 00 01", and (2) device software power down enabling "w 30 2e 80".

Table 45. Power Consumption in Software Power-Down Mode

Power-Down Mode	AVDD	SLVDD	SRVDD	HVDD	DVDD	IOVDD	TOTAL POWER
Voltage (V)	3.3	3.9	3.9	3.3	1.8	3.3	N/A
Current (µA)	0.20	0	0	0.20	1.10	2.10	N/A
Power (µW)	0.660	0	0	0.660	1.980	6.930	10.230

3 Conclusion

This application report discusses power consumption of the TLV320AIC31xx/DAC31xx audio converters. Scripts for different use cases are provided. The unused blocks of a specific-use case are turned down using register settings without any need for disconnecting external power supplies. The power measurement of this device goes lower than 10 mW for record and does not exceed 85 mW for record plus playback via both speakers and headphones. Using PLL for clock setting is optional for many processing blocks. This allows lower power consumption with a wide range of clock settings.

Revision History

Changes from Original (October 2010) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

Changes from A Revision (June 2014) to B Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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