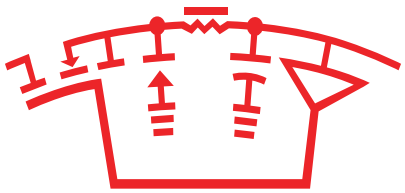

Power Supply Design Seminar

Introduction to the Trans-Inductor Voltage Regulator (TLVR)

Texas Instruments

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Topic 3
Matthew Schurmann and Mohamed Ahmed
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Introduced in 2019, the trans-inductor voltage regulator (TLVR) topology offers major transient response, power density and solution cost improvements (a >40% capacitor reduction for the design example reviewed in this topic) versus the traditional multiphase buck voltage regulator topology. This topic covers the operating principles of the TLVR topology, performance and cost improvements over traditional voltage regulators, design equations, and guidelines.

Introduction

Load transient regulation performance continues to be an important challenge in the design of voltage regulators for modern computing devices such as microprocessors, graphics processors, application-specific integrated circuits and field-programmable gate arrays. Technology trends in the development of these computing devices, such as rapidly increasing complexity, silicon process-node evolution, physical limitations of transistor scaling and chiplet architectures continue to accelerate the demands placed on the voltage regulators powering them. In some cases, high-end core-rail voltage regulators have thermal design currents greater than 1,000 A, peak currents greater than 2,000 A, rise times in the nanosecond range, and regulated output voltages of 0.7 V, ±3%.

The TLVR topology is derived from the multiphase half-bridge buck converter topology, but replaces the single-winding inductor of each phase with a two-winding coupled inductor, as shown in **Figure 1** and **Figure 2**. Similar to the multiphase buck converter, the primary side of each coupled inductor is connected between the switch node of each phase and the converter output voltage. The added secondary windings are connected in a series loop, with an additional inductor known as the compensating inductor (L_C). In the following sections, we'll discuss the limitations of the multiphase buck converter in terms of load transient response, fundamental operating principles of the TLVR topology, trade-offs and practical considerations.

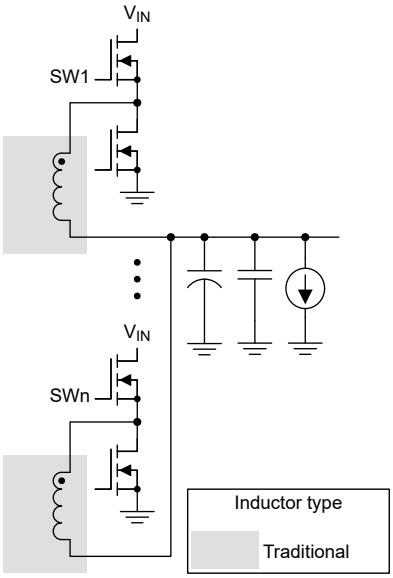


Figure 1. *Multiphase buck topology.*

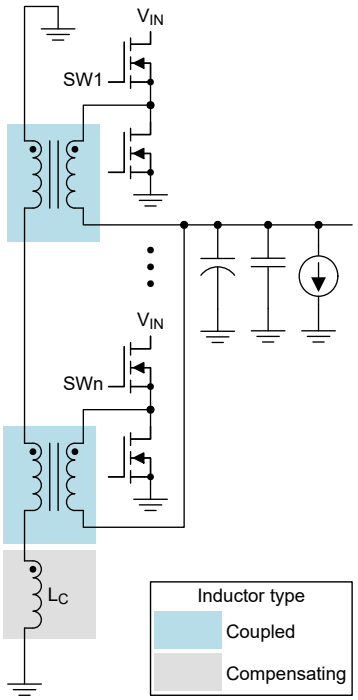


Figure 2. *TLVR topology.*

Converter Transient Response

Figure 3 shows a simple block diagram of a voltage regulator system subject to a load transient condition. I_{SUM} represents the sum of the individual inductor currents from each phase in the converter. I_{LOAD} represents the actual load current drawn by the load device. Any time I_{LOAD} changes, the voltage regulator responds by changing the effective duty cycle of switching in each phase in order for the I_{SUM} to ramp up or down to track the new I_{LOAD} value.

The output filter of the converter – in particular, the filter inductance – limits how quickly I_{SUM} can ramp to the new I_{LOAD} value. During the time when I_{SUM} is ramping up or down, the filter capacitors must supply the difference between them over time; this is known as the charge ΔQ. The output voltage of the converter will undershoot or overshoot during this time, and the only ways to limit the voltage deviation (ΔV) are to either increase the rate at which I_{SUM} can ramp (by reducing the filter inductance, for example) or to increase the total output capacitance (C_{OUT}) of the filter.

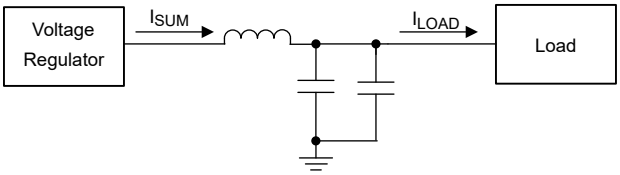


Figure 3. *Converter load transient block diagram.*

Figure 4 shows the typical I_{SUM} and output voltage waveforms in a traditional multiphase buck converter.

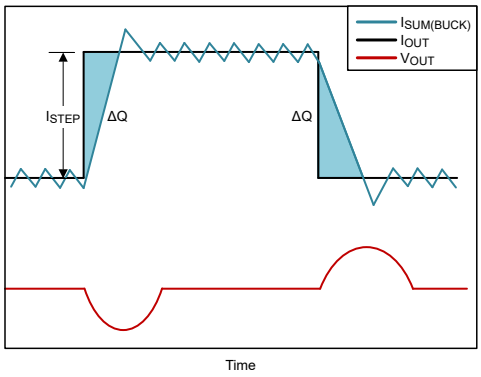


Figure 4. *Buck converter load transient.*

Equation 1 shows the relationship between the total output deviation ΔV, C_{OUT}, and the rate (slope) at which the converter can ramp its current up or down:

$$\Delta V = \frac{\Delta Q}{C_{out}} = \frac{\frac{1}{2} \times t_{resp} \times I_{step}}{C_{out}} = \frac{\frac{1}{2} \times \frac{I_{step}^2}{Slope}}{C_{out}} \quad (1)$$

For the traditional multiphase buck converter, this slope is directly related to the output filter inductance used for each phase. Reducing the inductance value would indeed improve the transient response of the converter.

Simply reducing the output inductance of each phase has unintended consequences for the converter's power losses and its steady-state ripple, however. Reducing the inductance value leads to a higher inductor current ripple and consequently a higher voltage ripple on the output of the converter, which typically also has stringent requirements. It also increases the root-mean-square (RMS) current in each phase, reducing overall converter efficiency.

In a multiphase buck converter topology, the inductance value is a constant, in both steady state and during transient events. Therefore, the selection of an inductance value is a balanced trade-off between transient response, power loss, and voltage ripple and current ripple. It is not practical to make the inductance very small; thus, a large amount of C_{OUT} may be required to limit ΔV in order to meet the specifications.

The TLVR topology addresses this problem by allowing a different effective filter inductance in different conditions. A high effective value of filter inductance during steady-state operation limits the converter ripple and RMS power losses. A low effective inductance value during transient conditions dramatically reduces the amount of C_{OUT} required to meet a given transient regulation specification. **Figure 5** shows the typical load transient response of a TLVR converter, having a much higher I_{SUM} slope during the converter response.

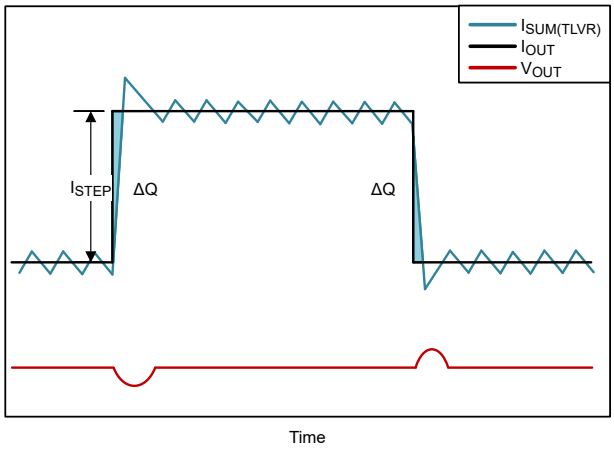


Figure 5. *TLVR load transient.*

It is possible to achieve a further reduction in capacitance with either the multiphase buck or TLVR topology using DC load line (DCLL), also known as adaptive voltage positioning. **Figure 6** demonstrates the concept. This technique applies to either the multiphase buck converter or TLVR topology and does not change fundamentally.

Given a specification, in terms of a load step size and minimum and maximum allowable output voltage, the converter typically regulates the output voltage to a constant value regardless of the load current – this is known as zero load line, R_{LL} = 0 mΩ. Then the allowed output voltage overshoot ($\Delta V_{overshoot}$) and undershoot ($\Delta V_{undershoot}$) each become equal to 50% of the total voltage specification window.

For a non-zero-load-line design, configure the converter to set its output voltage as a function of the sensed load current. The voltage at zero load (V_0) is configured to a value near the maximum allowed output voltage. **Equation 2** describes the output voltage when using the load line:

$$V_{OUT}(I_{OUT}) = V_0 - R_{LL} \times I_{OUT} \quad (2)$$

Equation 3 defines the R_{LL} value in terms of the allowed voltage change ΔV_{DROOP}:

$$R_{LL} = \frac{\Delta V_{DROOP}}{\Delta I_{STEP}} \quad (3)$$

Equation 4 and **Equation 5** express the effect of R_{LL} on the required C_{OUT} of the converter:

$$C_{OUT(\min,\ \text{step up})} = \frac{\Delta Q_{under}}{\Delta V_{under}} = \frac{\frac{1}{2} \times \frac{I_{STEP}^2}{Slope}}{\Delta V_{ac} + R_{LL} \times I_{step}} \quad (4)$$

$$C_{OUT(\min,\ \text{step down})} = \frac{\Delta Q_{over}}{\Delta V_{over}} = \frac{\frac{1}{2} \times \frac{I_{step}^2}{Slope}}{\Delta V_{ac} + R_{LL} \times I_{step}} \quad (5)$$

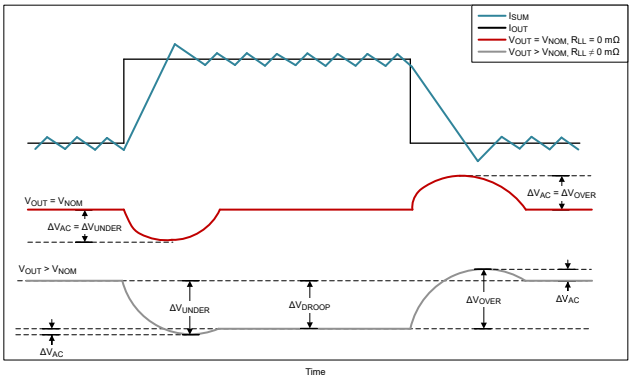


Figure 6. *DC load line, or adaptive voltage positioning.*

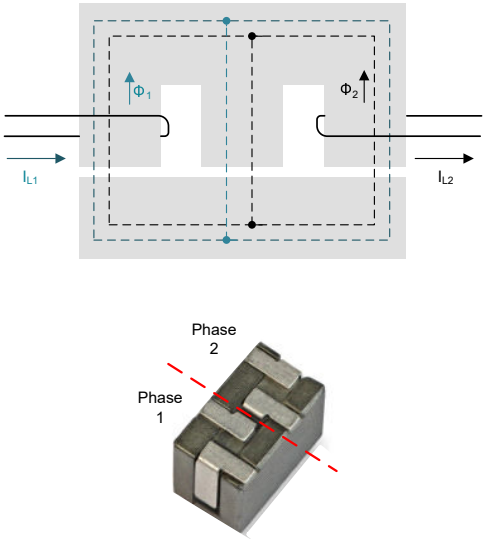
Magnetics

Because the TLVR topology achieves its transient benefits by allowing different effective inductance values in steady-state and transient conditions, it is helpful to explore the behavior of the coupled inductor structure that it uses. This concept is not entirely unique to the TLVR topology.

Figure 7 shows a traditional two-phase coupled inductor structure in which the windings for individual phases in the converter share a common magnetic core. Current in one winding directly induces current in the others, as the magnetic flux in the core is additive. During a load transient, a current change in one phase (one winding) directly causes a change in the same direction in the other phases. This behavior allows the total converter I_{SUM} to ramp up or down to meet the load current demand more quickly than if the phases were uncoupled.

The coupling coefficient (K) between different windings of this structure will typically be between 0.4 and 0.7. This coupling is well controlled by the core design (in **Figure 7**, by the air gap in the middle leg). Very high coupling

(K≅1.0) is not beneficial, as it increases the current ripple of the converter in steady state. Very low coupling simply reduces the transient benefits achievable.

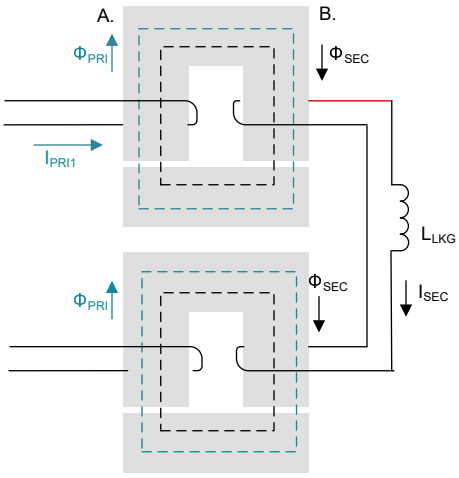


Source: Eaton

Figure 7. *Traditional two-phase inverse-coupled inductor.*

Adoption of the traditional coupled inductor for high-phase-count designs (more than four phases) has been limited for several reasons. Extending it to higher phase counts requires a complex core geometry to maintain coupling symmetry. This structure also requires more customization of inductors for different designs, limiting scalability; for example, you would need a different inductor for two- and three-phase designs. Additionally, until recently, aggressive patent protection limited multisourcing options; no such limitation exists for the TLVR topology.

The TLVR topology relies on a similar principle but with a different magnetic structure, known as an indirect-coupled inductor, shown in **Figure 8**. Each phase inductor has its own physical core with two windings, so this structure is easily scalable to higher phase counts simply by adding more cores. The magnetizing inductance (L_M) of each coupled inductor provides energy storage and filtering. The K between two windings on one core can be very high. Passing the same secondary-side current to all phases achieves coupling between cores (the phases), as they are connected in a loop.



A. Primary side (connect to power stage)

B. Secondary side (provides coupling)

Figure 8. *Indirect-coupled two-phase inductor.*

Similar to a traditional coupled inductor, it is beneficial to have the coupling coefficient (α) between phases in the range of 0.4 to 0.7. The secondary loop controls this coupling. The inductance in the secondary loop may be very low, leading to high coupling (and thus a large steady-state current ripple) or simply not well-controlled, as a result of interconnect and physical construction tolerances.

To control the coupling between phases, the TLVR topology often uses a separate physical inductor on the secondary side, L_C, shown in **Figure 9**. If the leakage inductance in the secondary-side loop is large enough compared to the magnetizing inductance of the individual coupled inductors, and can be well-controlled by manufacturing, a separate physical L_C is not needed, especially in high-frequency designs switching at higher than 1 MHz per phase.

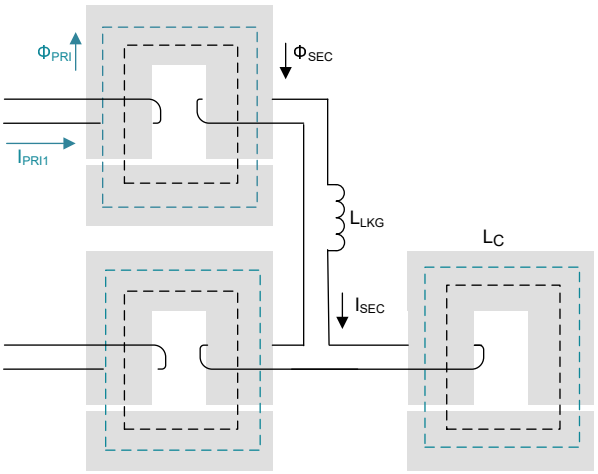
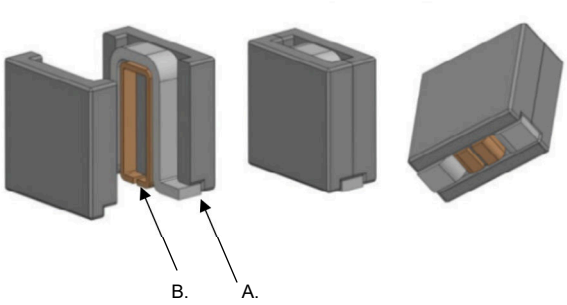


Figure 9. *Indirect-coupled two-phase inductor with a physical compensating inductor.*

Figure 10 shows the typical construction of a TLVR inductor. The inductor size and shape are similar to traditional high-current ferrite core inductors for multiphase buck converters, with the secondary winding inside the primary winding. The land pattern on the bottom of the package enables co-layout with both TLVR and non-TLVR designs on the same physical printed circuit board (PCB).



A. Primary winding

B. Secondary winding

Source: Eaton

Figure 10. *Typical TLVR inductor construction.*

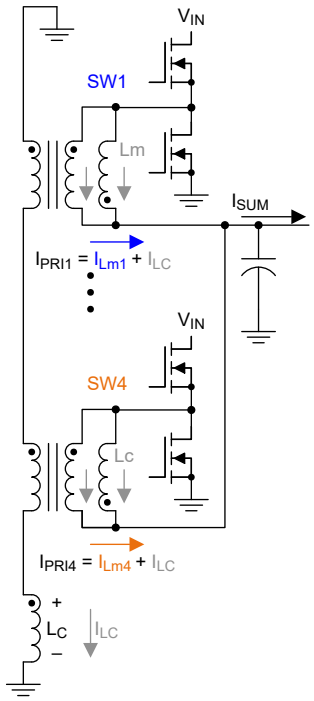
TLVR Topology Operating Principles

Steady-State Operation

Figure 11 shows a typical TLVR converter schematic, with important nodes, voltages and currents labeled. **Figure 12** illustrates the steady-state operating waveforms of a TLVR converter, with four phases shown. In this example, the pulses from adjacent phases do not overlap in time. There is no maximum duty-cycle requirement for the TLVR topology. The same principles apply for higher-duty-cycle applications where pulses do overlap in time.

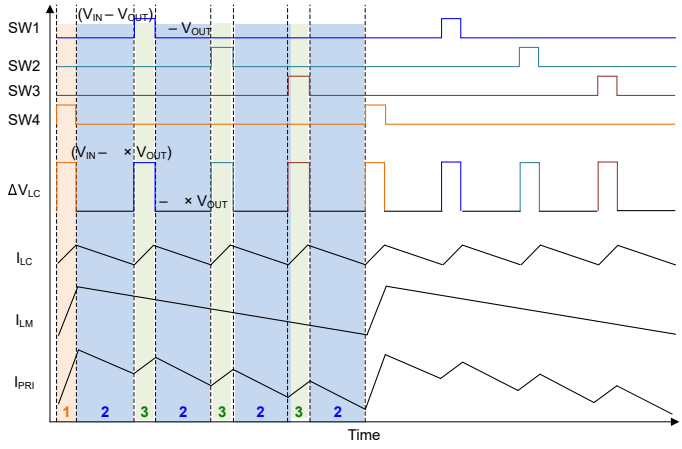
Figure 12 shows the voltage and current waveforms of the L_C of the secondary-side loop, switch nodes of all four phases, and the primary-side current of phase 4 (I_{PRI4}). For clarity, this figure includes labels for the three distinct states of operation.

The most important relationships are those of the L_C loop and its influence on I_{PRI} and I_{SUM}.



Four-phase example, no pulse overlap

Figure 11. *Steady-state topology.*



Four-phase, no pulse overlap

Figure 12. *Steady-state waveforms.*

The magnetizing voltage for each phase is similar to that of a buck converter. **Equation 6** applies to phase on, and **Equation 7** applies to phase off. The magnetizing inductance always follows the fundamental inductor relationship shown in **Equation 8**:

$$\Delta V_{Lm,i} = V_{IN} \quad (6)$$

$$\Delta V_{Lm,i} = V_{IN} - V_{OUT} \quad (7)$$

$$I_{LM} = \frac{\Delta V_{Lm}}{L_m} \quad (8)$$

The voltage across the L_C is always equal to the sum of the magnetizing voltages across all phases, as shown in **Equation 9**. L_C itself always follows the fundamental inductor relationship, expressed by **Equation 10**:

$$\Delta V_{LC} = V_{Lm1} + V_{Lm2} + \ldots \quad (9)$$

$$I_{LC} = \frac{\Delta V_{LC}}{L_C} \quad (10)$$

The I_{PRI} for each phase is equal to the sum of its magnetizing current and $I_{LC,}$ expressed in **Equation 11**. I_{SUM} is the sum of the primary currents from all phases, expressed by **Equation 12**:

$$I_{PRI,i} = I_{Lm,i} + I_{LC} \quad (11)$$

$$I_{SUM} = I_{PRI1} + I_{PRI2} + \ldots \quad (12)$$

Table 1 summarizes the state of each of the relevant voltages and currents shown in **Figure 12**, with respect to the derivation of I_{PRI4} shown in the plot.

Parameter	State 1 Phase 4 on, phases 1, 2 and 3 off	State 2 All phases off	State 3 Phase 4 and two others off, one of the other phases is on
V_{SW1}	0 V	0 V	One phase is equal to V_{IN} and the other two are equal to 0 V.
V_{SW2}	0 V	0 V	
V_{SW3}	0 V	0 V	
V_{SW4}	V_{IN}	0 V	$-V_{OUT}$
ΔV_{LM1} (1)	$-V_{OUT}$	$-V_{OUT}$	One phase is equal to $V_{IN} - V_{OUT}$ and the other two are equal to $-V_{OUT}$
ΔV_{LM2} (1)	$-V_{OUT}$	$-V_{OUT}$	
ΔV_{LM3} (1)	$-V_{OUT}$	$-V_{OUT}$	
ΔV_{Lm4}	$V_{IN} - V_{OUT}$	$-V_{OUT}$	$-V_{OUT}$
I_{Lm4}	Increasing(2)	Decreasing(2)	Decreasing(2)
ΔV_{LC}	Sum of V_{SW1} to V_{SW4} (5)	Sum of V_{SW1} to V_{SW4} (5)	Sum of V_{SW1} to V_{SW4} (5)
I_{LC}	Increasing(3)	Decreasing(3)	Increasing(3)
I_{PRI4}	Increasing(4)	Decreasing faster(4)	Decreasing slower(4)

Table 1. *Four-phase example, steady-state voltages and currents.*

(1) Not in **Figure 12**.
(2) $\Delta V_{LM4}/L_M$
(3) $\Delta V_{LC}/L_C$
(4) $I_{LM4} + I_{LC}$
(5) $V_{IN} - 4 \times V_{OUT}$

Load Transient Step-Up

Figure 13 and **Figure 14** show a simulated comparison between a multiphase buck converter and a TLVR design under the same load step-up condition. **Table 2** summarizes the simulation parameters. These are closed-loop simulations using the TI TPS536C9T DCAP+™ constant on-time controller.

A few observations about **Figure 13** and **Figure 14**:

- The TLVR design responds to the transient (I_{SUM} catches up to I_{LOAD}) much more quickly because the I_{SUM} rises at a faster rate. As a consequence, the output voltage deviation is significantly lower.

- During the transient response, the multiphase buck converter design required many more pulses to respond than the TLVR design, meaning that the TLVR design delivers more energy per pulse during the transient event.
- Given the nature of constant-on-time control, pulses overlapped during the transient response. The L_C voltage increased to a level significantly higher than the input voltage during pulse overlap operation, then returned to normal operation at steady state.

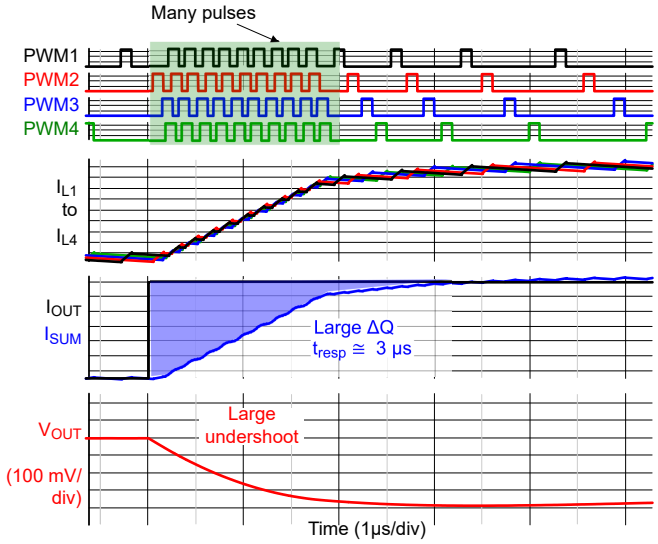


Figure 13. *Multiphase buck converter.*

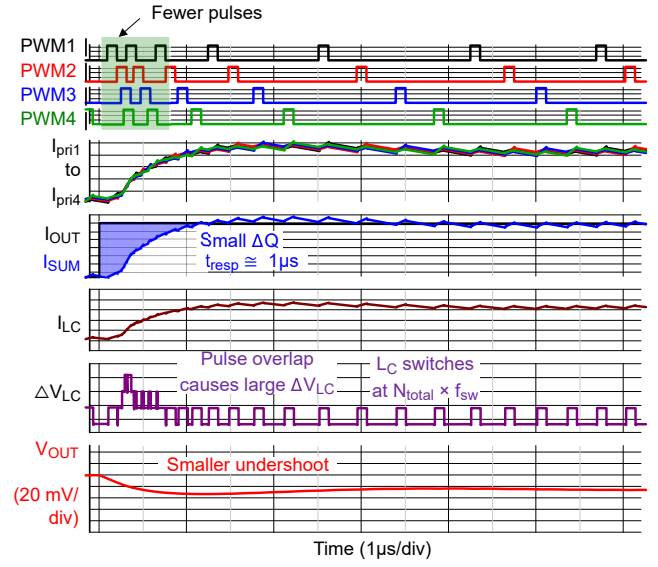


Figure 14. *TLVR.*

Parameter	Description	Value
V_{IN}	Input voltage	12 V
V_{OUT}	Output voltage	0.8 V
N_{TOTAL}	Total operating phase number	4 phases
f_{SW}	Switching frequency per phase	600 kHz
I_{STEP}	Load step size	25 A to 325 A, instantaneous
L_M/L_{BUCK}	Magnetizing inductance L_M for TLVR, filter inductor L_{BUCK} for buck	150 nH/150 nH
L_C	L_C value for TLVR	180 nH
C_{OUT}	Output capacitance	5.0 µF, idealized

Table 2. *Simulation parameters for transient load step-up and step-down examples.*

Following the relationships described in the **Steady-State Operation** section, it is evident why the TLVR is able to ramp its I_{SUM} up more quickly than the buck converter, and why its transient response was superior.

I_{SUM} for the buck converter is simply the sum of its individual inductor currents, as shown in **Equation 13**. For the TLVR design, I_{LC} gets added once for each phase, in addition to each magnetizing current (I_{LM}), as shown in **Equation 14**:

$$I_{SUM(buck)} = I_{L1} + I_{L2} + \ldots \quad (13)$$

$$I_{SUM(TLVR)} = I_{PRI1} + I_{PRI2} + \ldots = (I_{Lm1} + I_{Lc}) + (I_{Lm2} + I_{Lc}) + \ldots \quad (14)$$

All inductors in the system follow the fundamental inductor relationship. During the transient response to the load step-up, the converter turns on N_{ON} phases simultaneously. For various reasons, it may not be possible to turn on all phases at once, so also consider that N_{OFF} phases remain off at any one time. **Equation 15** and **Equation 16** show the rising I_{SUM} slope for the multiphase buck converter. These equations do not account for the controller response time, but show only the limitation from the converter topology.

$$\uparrow Slope_{(buck)} = \frac{\Delta V_{L1}}{L} + \frac{\Delta V_{L2}}{L} + \ldots \quad (15)$$

$$\uparrow Slope_{(buck)} \cong N_{ON}\left(\frac{V_{IN} - V_{OUT}}{L}\right) - N_{OFF}\left(\frac{V_{OUT}}{L}\right) \quad (16)$$

Equation 17 and **Equation 18** show the rising I_{SUM} slope for the TLVR design, assuming that the TLVR magnetizing inductance L_M was equal to the buck filter inductor L for comparison purposes:

$$\uparrow \text{Slope}_{(\text{TLVR})} = \left(\frac{\Delta V_{L1}}{L_M} + \frac{\Delta V_{LC}}{L_C}\right) + \left(\frac{\Delta V_{L2}}{L_M} + \frac{\Delta V_{Lc}}{L_C}\right) + \ldots \quad (17)$$

$$\uparrow \text{Slope}_{(\text{TLVR})} \cong \uparrow \text{Slope}_{(\text{buck})} + N_{TOTAL} \times \left(\frac{N_{ON} \times V_{IN} - N_{TOTAL} \times V_{OUT}}{L_C}\right) \quad (18)$$

Written in this way, the additional terms clearly show the influence of I_{LC} in enabling the TLVR design to respond more quickly to transients than a traditional multiphase buck design.

Load Transient Step-Down

Figure 15 and **Figure 16** show a simulated comparison between a multiphase buck converter and a TLVR design under the same load step-down condition. This simulation uses the same parameters as those in **Table 2**.

A few observations about **Figure 15** and **Figure 16**:

- The TLVR design responds to the transient (I_{SUM} catches up to I_{LOAD}) much more quickly because the I_{SUM} is falling at a faster rate. As a consequence, the output voltage deviation is significantly lower.
- In this case, both designs had the same number of phases off, but the TLVR design ramped down the I_{SUM} at a faster rate.

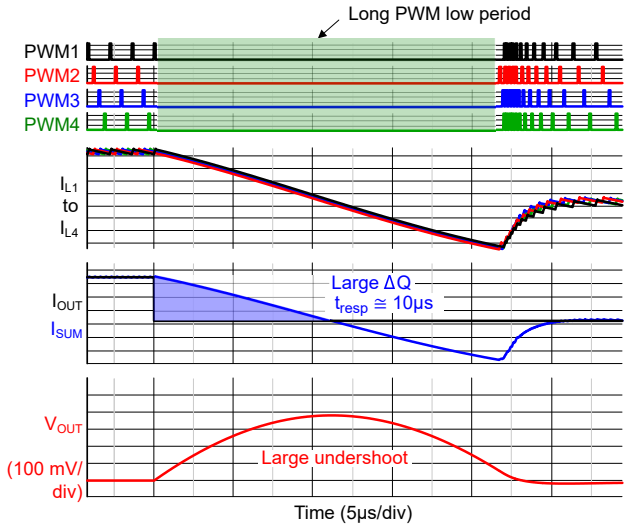


Figure 15. *Multiphase buck converter.*

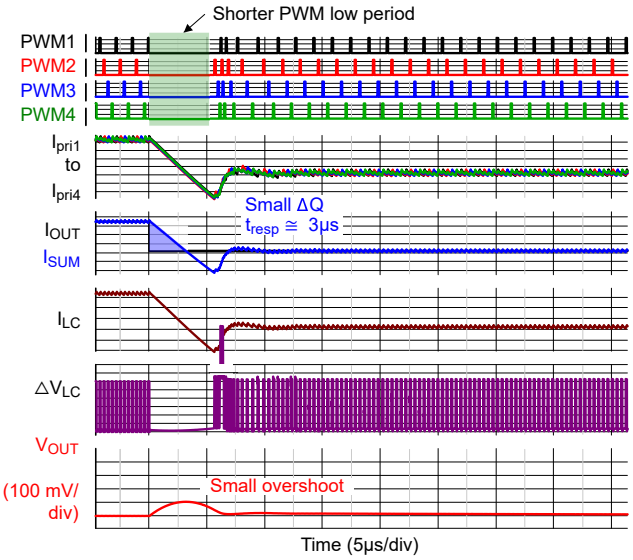


Figure 16. *TLVR.*

Again, the relationship of I_{LC} to I_{SUM} explains the superior transient response of the TLVR design. And again, all inductors in the system follow the fundamental inductor relationship. During the transient response to the load step-down, the converter turns off all phases, N_{TOTAL}, simultaneously. **Equation 19** shows the falling I_{SUM} slope for the multiphase buck converter:

$$\downarrow \text{Slope}_{(\text{buck})} = -N_{TOTAL}\left(\frac{V_{OUT}}{L}\right) \quad (19)$$

Using a similar analysis, **Equation 20** shows the falling I_{SUM} slope for the TLVR design, assuming that the TLVR magnetizing inductance L_M is equal to the buck filter inductor L for comparison purposes. The TLVR design ramps down its I_{SUM} faster given the factor from the L_C loop, which decreases proportionally to the square of the number of phases, N_{TOTAL}.

$$\downarrow Slope_{(TLVR)} \cong \downarrow Slope_{(buck)} - N_{TOTAL} \times \left(\frac{N_{TOTAL} \times V_{OUT}}{L_C}\right) \quad (20)$$

L_C Inductor Selection

The L_C has somewhat unique requirements compared to other inductors in a typical DC/DC design. The inductance of L_C is a trade-off between current ripple and transient response benefits. Typically, start with $L_C = L_M$ as a balanced trade-off. Values between 0.8 to 1.5 times L_M are common with discrete designs. Lower values may be more common in highly integrated designs, such as power modules.

At steady state, L_C carries no DC current – only a small AC current ripple – because it is switching at a high frequency (at least $N_{TOTAL} \times f_{SW}$ when there is no pulse overlap). Its current ripple dominates its RMS current at steady state, described in **Equation 21**. Consider low core-loss materials, such as ferrite cores, because of the high f_{SW}. Another option to further improve transient response may be soft-saturating cores.

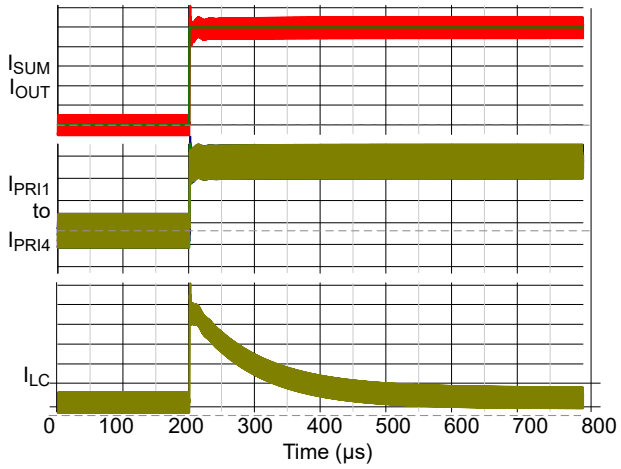
$$I_{rms(L_C)} \approx \frac{\Delta I_{Lc}}{\sqrt{3}} \quad (21)$$

However, L_C can continue to build large amounts of current during transient events, as expressed by **Equation 22**, where t_{RESP} is the response time of the controller, as highlighted in **Figure 15** and **Figure 16**. Therefore, size the L_C with a high saturation current, similar to the coupled inductors used in each phase.

$$I_{SAT(L_C)} \gg t_{RESP} \times \left(\frac{N_{ON(step)} \times V_{IN} - N_{TOTAL} \times V_{OUT}}{L_C}\right) \quad (22)$$

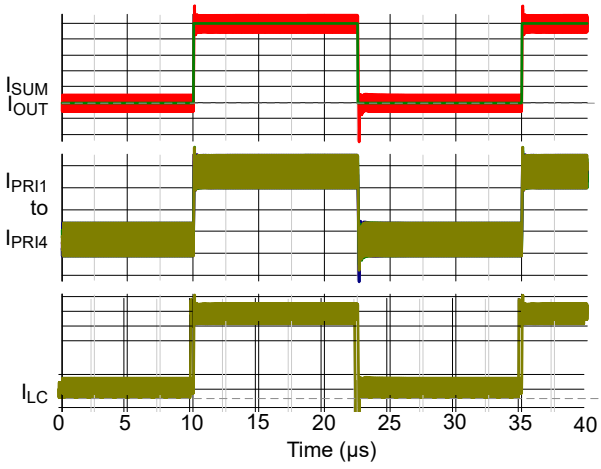
After building up a large current, the L_C current naturally decays to zero, with a relatively high time constant, τ_{LC}, as described in **Equation 23**, formed by the L_C and the resistances in the L_C loop. During high-frequency repetitive transients, I_{LC} may not settle fully but will not saturate, as load steps up and down push I_{LC} in different directions. **Figure 17** and **Figure 18** show a simulation of this behavior:

$$\tau_{L_C} = \frac{L_C}{R_{DCR,L_C} + N_{total} \times R_{DCR,secondary} + R_{routing}} \quad (23)$$



f_{SW} < 1 kHz

Figure 17. *Low-frequency transient event.*



f_{SW} = 65 kHz

Figure 18. *High-frequency transient event.*

The voltage across the L_C, ΔV_{LC}, can exceed the input voltage, V_{IN}, during a load step response. Assuming that a controller turns on N_{ON} phases in response to the load step, **Equation 24** calculates ΔV_{LC}:

$$\Delta V_{LC(max)} = N_{ON(step)} \times V_{IN} - N_{TOTAL} \times V_{OUT} \quad (24)$$

Creepage is not generally a concern, as the high voltage is not sustained for a long period of time. But the high transient voltage across L_C may be important to know for application safety and component reliability in some cases.

Steady-State Ripple

TLVR-based designs tend to have larger output voltage ripple than their multiphase buck converter counterparts. Normally, multiphase converters have low voltage ripple caused by interleaving and ripple cancellation. The converter achieves optimum ripple cancellation when each inductor current has a phase offset of 360 degrees/N_{TOTAL} with respect to each other. For TLVR designs, however, I_{LC} gets added once to I_{SUM} for each phase offset. So while the I_{SUM} contribution from each magnetizing inductance I_{LM} does cancel because of interleaving, the contribution from I_{LC} does not, as expressed by **Equation 25**:

$$I_{SUM(TLVR)} = (I_{Lm1} + I_{Lc}) + (I_{Lm2} + I_{Lc}) + \ldots \quad (25)$$

Figure 19 illustrates the relationship between the ripple on I_{SUM} and the ripple on the converter output voltage. Typically, the converter and load are separated by a power distribution network (PDN). I_{SUM} is generated by the converter in one location and fed to the PDN, at some distance. The impedance of the PDN (including output capacitors) then determines the output voltage ripple. For this reason, the additional I_{SUM} ripple in TLVR designs translates directly to a larger output voltage ripple.

An example in **Figure 20** demonstrates the influence of the converter duty cycle. The I_{LC} ripple can still become very small at certain duty cycles, when phases overlap perfectly (with $N_{TOTAL} \times D = 1, 2, \ldots$). However, for typical applications (highlighted in **Figure 20** for typical output voltages of 1.0 V, 1.2 V and 1.8 V), TLVR designs typically have a 25% to 50% larger I_{SUM} ripple, and consequently, a 25% to 50% larger output voltage ripple. For many cases this will not be an issue, because the C_{OUT} required to meet the transient requirement is much larger than the capacitance required to meet the design's ripple requirement.

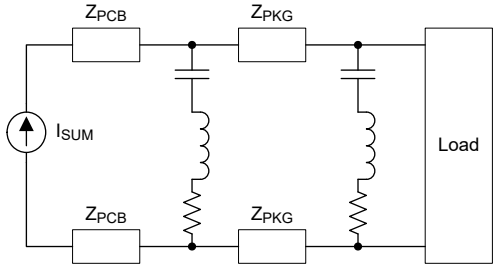
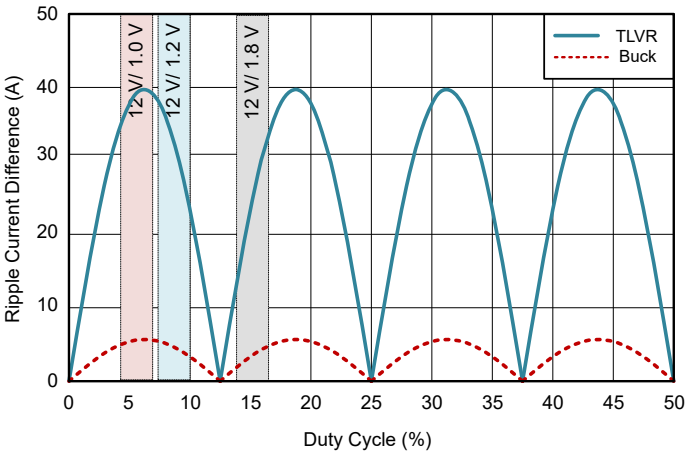


Figure 19. *Model for output voltage ripple.*



8 phases — L_M = 150 nH

L_C = 120 nH — $L_{VR} = L_{eq}$ = 125 nH

Figure 20. *Output voltage ripple.*

A common technique to reduce the voltage ripple of a TLVR design is to use more than one L_C loop. **Figure 21** shows an example with two L_C loops. The phase-fire order for each phase is such that the I_{LC1} and I_{LC2} currents are 180 degrees out of phase, allowing the I_{LC1} and I_{LC2} current ripple to cancel.

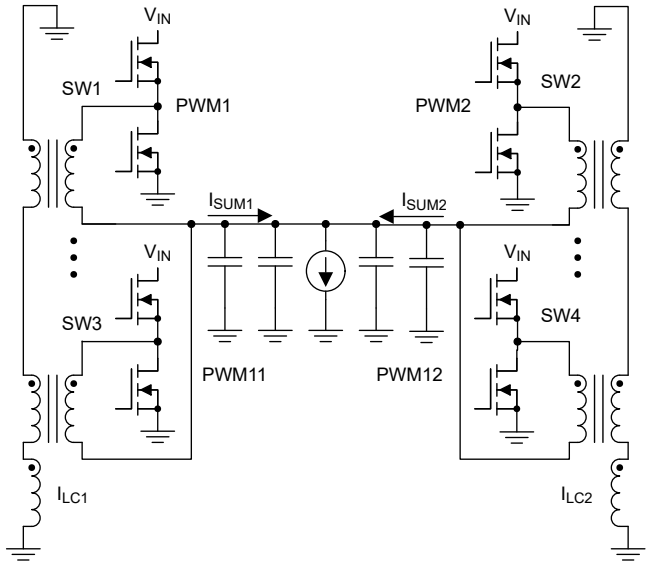


Figure 21. *Interleaved TLVR design.*

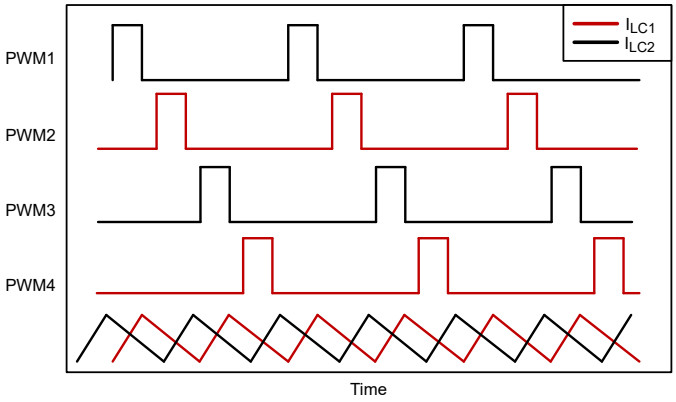


Figure 22. *Two-loop interleaved TLVR waveforms.*

Interleaving is also common in cases where space constraints on the board layout prevent placing phases near each other. Phases on each L_C loop are co-located with each other, but the L_C loops may be separated by some distance, sometimes even on different sides of the load device. While less beneficial in terms of output voltage ripple, TLVR designs with asymmetric phase numbers on each L_C loop are also possible.

Power Loss and Efficiency

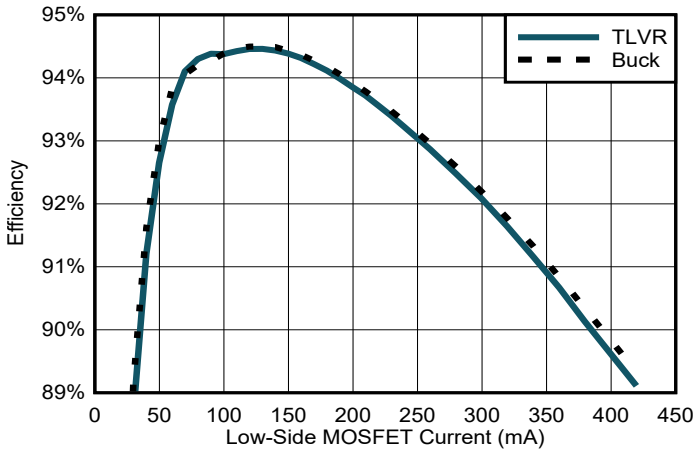
Figure 23 compares the power efficiency between a multiphase buck converter and TLVR when designed with the same component values. The curves are already quite similar, but the TLVR design is a small amount lower (0.1%) in terms of efficiency.

While this plot is useful for demonstration purposes, typically, multiphase buck and TLVR designs will not have the same inductance values. The buck converter will require a lower inductance value to meet the same transient specifications, which further reduces its power efficiency. In practice, when designing two converters to the same specifications, the multiphase buck and TLVR converters have approximately equivalent efficiency. In some cases, TLVR designs can have slightly higher efficiency.

Two loss mechanisms differentiate the TLVR design from the multiphase buck converter. Most obviously the L_C loop losses are present only in TLVR designs. Earlier, **Equation 21** showed the RMS current in the L_C loop, as a result of its current ripple. Thus, the losses in the L_C loop have a component of RMS conduction losses, as well as core losses, which may be significant given the high switching frequency of the L_C. Equation 25 estimates the power losses in the L_C loop:

$$P_{Lc} \cong I^2_{rms(L_C)} \times \left(R_{DCR,L_c} + N_{TOTAL} \times R_{DCR,secondary} + R_{routing}\right) + P_{core(L_C)} \quad (26)$$

Additionally, consider that the additional ripple from I_{LC} will increase the RMS current in each power stage, and thus the conduction losses. **Figure 24** demonstrates how the addition of I_{LC} increases the peak-to-peak current ripple, ΔI_{PP}, in the low-side switch of each phase. As the I_{LC} current ripple increases with lower phase numbers, this additional component can become significant. That is one reason why TLVR designs are typically reserved for high-power, high-phase-count (greater than six phase) designs.



V_{IN} = 12 V

V_{OUT} = 1.80 V

f_{SW} = 600 kHz

R_{LL} = 0.5 mΩ

$L_M = L_{BUCK}$ = 120 nH

L_C = 120 nH

Excludes PDN conduction losses

Figure 23. *Efficiency vs. output current.*

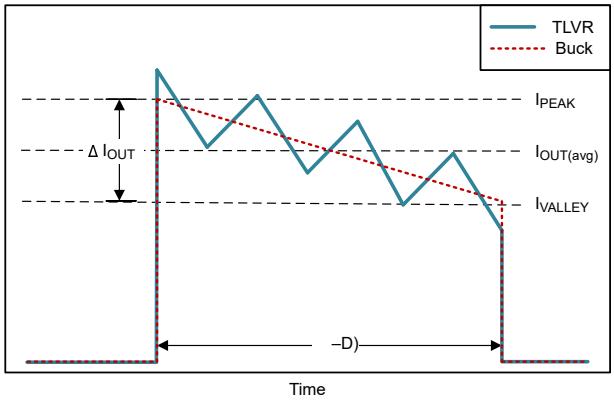


Figure 24. *Addition of I_{LC} to low-side metal-oxide semiconductor field-effect transistor (MOSFET) current.*

To understand this loss mechanism, **Equation 27** expresses the relationship between the current ripple and low-side MOSFET RMS current for a typical buck converter design. An exact equation for the TLVR design is more complex, but the buck converter equation demonstrates the influence of ΔI_{PP}.

$$I_{RMS(LSFET)} = I_{OUT} \times \sqrt{1-D} \times \sqrt{1+\frac{1}{3}\times\left(\frac{\Delta I_{PP}}{2\times I_{OUT}}\right)^2} \quad (27)$$

It is also common to use dynamic phase shedding (DPS) in high-phase-count designs to improve light-load efficiency. Switching a fewer number of phases when the total output current is low enough to be supported without all phases active reduces switching losses. Phases can be in one of three states: high-side MOSFET on, low-side MOSFET off; high-side MOSFET off, low-side MOSFET on; or both MOSFETs off. Typically, nonlinear control techniques add or drop phases quickly during load transient events, so the impact on the load transient response is minimal. **Figure 25** shows the current flow in each state.

In a TLVR design, the L_C loop continues to conduct current through the body-diode phases in the third state (both MOSFETs off), which are not switching. There will be additional power losses from nonswitching phases caused by the voltage drop of the body diodes, V_{diode}. Therefore, for phase shedding to make sense, the switching losses saved by not switching a phase must be greater than that created by the body-diode losses. **Equation 28** describes the power losses in nonswitching phases:

$$P_{cond,\,HiZ} = I_{LC(rms)} \times V_{diode} \quad (28)$$

A measured plot of the same design with phase shedding on and off, shown in **Figure 26**, demonstrates the TLVR design efficiency improvement at light load.

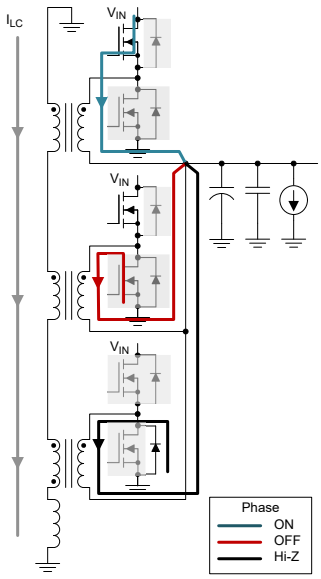
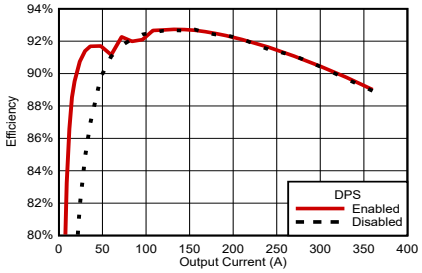


Figure 25. *Dynamic phase shedding.*



V_{IN} = 12 V	V_{OUT} = 1.80 V
f_{SW} = 90 kHz	$L_M = L_C$ = 100 nH
8 phases	Dual-side layout
TLVR	CSD08860 (90-A SPS)

Figure 26. *Efficiency vs. output current.*

Phase Multiplication

As power requirements continue to increase rapidly, it is often necessary to design very high phase-count (more than 16 phase) designs using controller devices that do not have enough independent pulse-width modulation (PWM) outputs to control each phase individually. It has become common to phase double or phase multiply – that is, to drive more than one power stage with the same controller PWM output. This practice enables easy scalability of multiphase designs – buck converter or TLVR – to high power levels.

Figure 27 shows the connections of the L_C loops in an interleaved, phase-doubled TLVR design. Such a design could, for example, extend a 12-phase design to 24 or 36 phases, without requiring a different controller device. For all phases (doubled or not) in the same L_C loop, the secondary sides are connected in series. The current feedback lines from each phase (not shown in **Figure 27**) can be resistor-averaged for power stages with voltage-source-output current sensing, or simply added for power stages with current-source-output current sensing. It is possible to connect temperature sense outputs from each power stage (also not shown in **Figure 27**) together, regardless of which L_C loop the power stages are in.

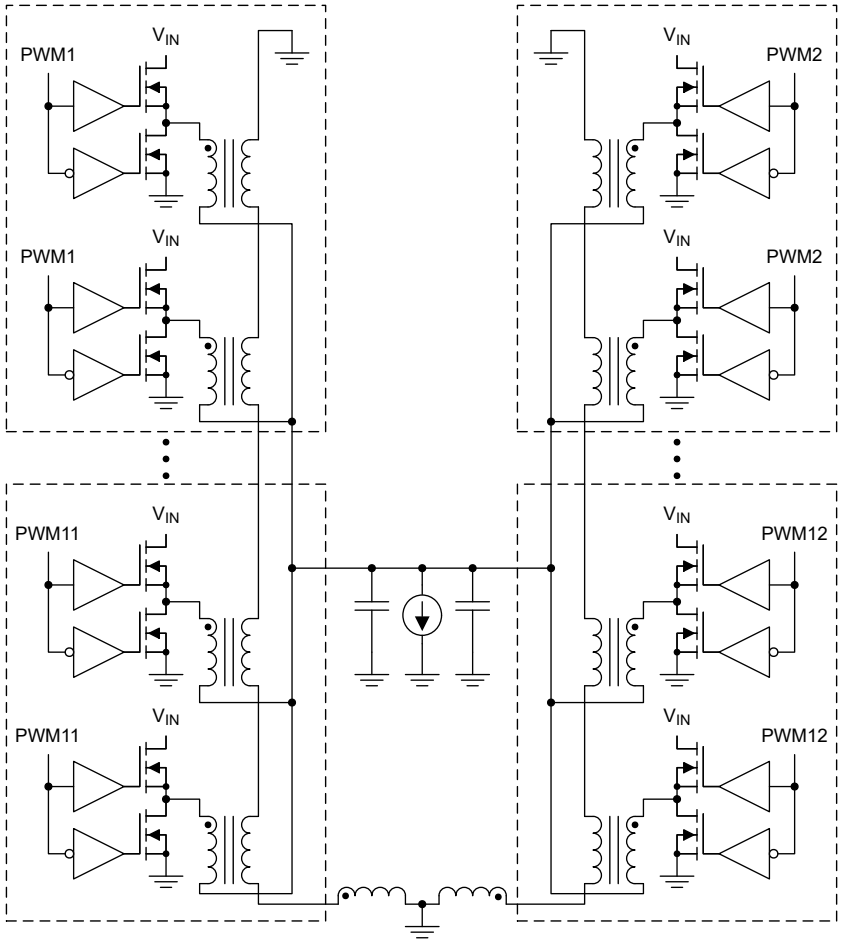


Figure 27. *Interleaved phase-doubling TLVR topology.*

PCB Layout

Figure 28 shows an example circuit board layout and component placement for a TLVR design powertrain. This design uses 4-mm-by-6-mm power-stage devices and co-layout-compatible TLVR inductors, enabling similar placement to a typical multiphase buck design.

The L_C loop runs through the middle of the primary-side pads. The secondary-winding pads of the TLVR inductor enable the running of this loop to occur on the top layer, without requiring many vias or wide traces. Because the L_C loop can conduct high current during transient events, the traces are as wide as the clearance rules allow, but multilayer planes are not required. Inner ground planes close the L_C loop from one side of the powertrain to another. Sensitive circuitry should have a wide clearance to the L_C, and L_C loop traces to avoid noise coupling and interference.

The L_C inductor is placed to the side of the power stages. Because the L_C can be subjected to voltages higher than V_{IN} and will be switching at a high frequency, high transient voltages and electromagnetic interference may become a concern as well. One possibility to mitigate this (not shown in **Figure 28**) is to split the L_C into two physical inductors – each with an inductance of one-half L_C – and place them symmetrically on either side of the power stages. This lowers the maximum voltage across each L_C during transient events.

Placing the phases as close to each other as possible saves space. However, the phase-fire order is not sequential. Changing the phase-fire order helps to reduce crosstalk issues between phases by spreading their switching nodes out from each other in the time domain.

Figure 29 is a zoomed-out example of a high-phase-count layout design that uses two L_C loops, placing doubled phases next to one another and in the same L_C loop. The phases and L_C in each loop follow the example in **Figure 28**. The loops are placed on opposite sides (sometimes referred to as cardinal directions, east and west) of the load to minimize the PDN routing between the output of each inductor and the pins of the load device. Two sides of the load device remain open, on the top side, for high-frequency signal routing, as needed by the design.

Decoupling capacitors (not shown in **Figure 29**) are under and, if possible, inside the footprint of the load device. There are placeholders for polymer bulk capacitors, but some designs will not need them. Placing the controller device far away from the powertrain avoids noise issues, with long traces connecting it to the power stages in each L_C loop. As with any high-power design, it's important to maintain good signal integrity on the PWM outputs, current-sense inputs and voltage-sense lines for the controller.

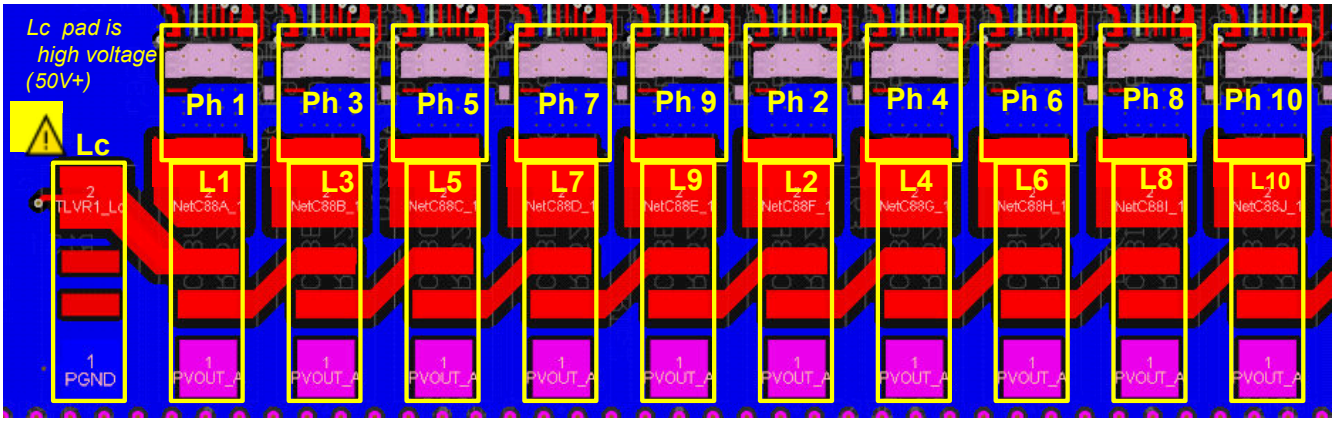


Figure 28. *Example TLVR powertrain layout.*

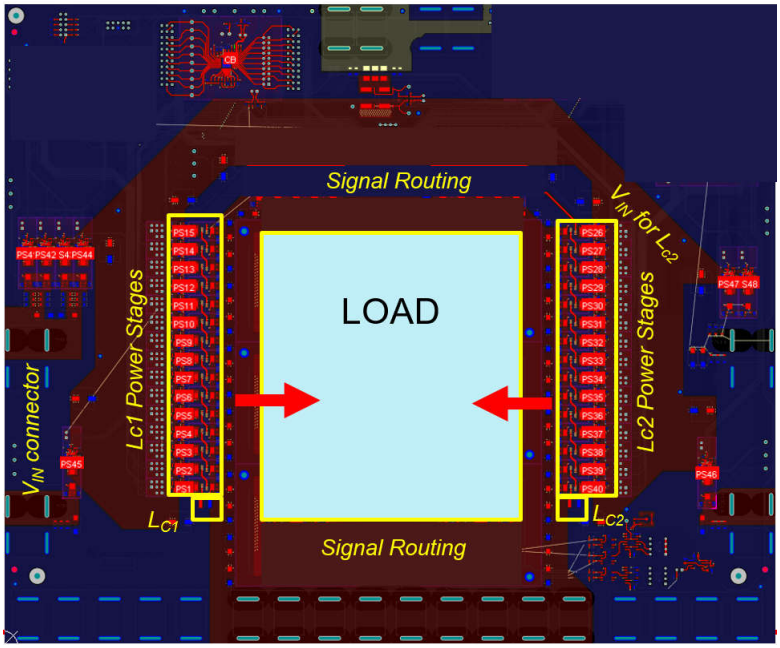


Figure 29. *Example phase-doubled interleaved TLVR layout.*

TLVR-Optimized Components

Recently, semiconductor vendors such as Texas Instruments (TI) have begun to offer multiphase controllers and power stages optimized for TLVR designs.

Smart power stages optimized for TLVR designs require higher-bandwidth current-sensing architectures because of the high-speed nature of the TLVR topology. The IOUT pin waveform of a TI smart power stage, for example, tracks even the induced current ripple from the L_C loop in a TLVR design. This requires current-sensing bandwidth at least an order of magnitude higher than the f_{SW} of the design on a per-phase basis. The TLVR topology also increases the bandwidth requirements for high-speed overcurrent protection.

Smart power stages optimized for TLVR designs must also be rated for increasingly high RMS currents and be able to support peak current pulses nearly two times their RMS rating for short durations, thermally as well as electrically.

Controllers generally do not need re-architecting. TLVR designs use the same control schemes designed for multiphase buck designs. TI controllers continue to use the DCAP+ control architecture, a form of constant on-time valley current-mode control. They may still require second-order optimizations such as new gain and compensation parameters suited to the TLVR powertrain. Higher-strength PWM output drivers are often needed to support longer distances between multiple L_C loops while maintaining good signal integrity. The implementation of a new protection mechanism for an open or shorted L_C loop should ease manufacturability concerns.

Table 3 and **Table 4** summarize TLVR-optimized components available from TI at the time of this writing, with more under development.

Part number	Current rating	Package size (mm)	I_{MON}
CSD95440	80-A peak, 40-A RMS	5 × 6	Voltage
CSD95510	90-A peak, 50-A RMS	4 × 6	Voltage
CSD95560	90-A peak, 50-A RMS	4 × 6	Current
CSD95520	60-A peak, 30-A RMS	4 × 5	Voltage
CSD95570	60-A peak, 30-A RMS	4 × 5	Current

Table 3. *TLVR-optimized smart power stages.*

Part number	Phases	Package size (mm)	Interface
TPS53685	8	5 × 5	AMD
TPS536C5	12	6 × 6	AMD
TPS53689T	8	5 × 5	Intel
TPS536C9T	12	6 × 6	Intel

Table 4. *TLVR-optimized controllers.*

Example Side-by-Side Design

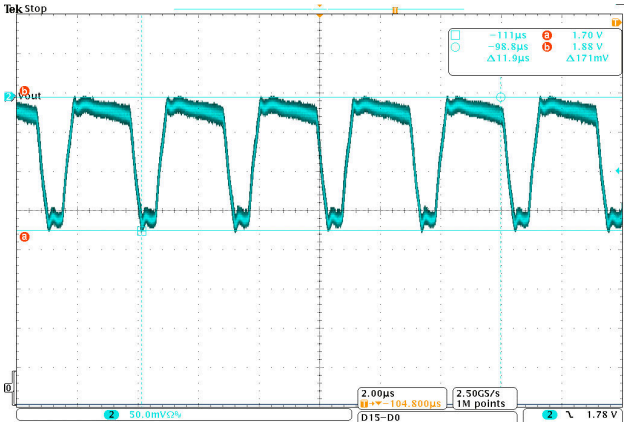
The examples in earlier sections demonstrated the difference between a multiphase buck design and a TLVR design with the same external components. This comparison is not often practical, however, because the requirements of the load do not change – it is the design that must change to meet the load requirements. As we've discussed, TLVR inductors are footprint-compatible with standard single-winding inductors, enabling the testing of both designs with the same physical PCB layout.

Table 5 summarizes one such example. The TLVR design met the same specifications as the multiphase buck converter design with almost no impact on overall power losses, and an over 40% reduction in C_{OUT} required.

Figure 30 and **Figure 31** illustrate the worst-case overshoot waveforms for this design.

Parameter	Multiphase buck	TLVR
Controller/standby power supply	TPS53689, CSD95440	
Input voltage (V_{IN})	12 V	
Output voltage (V_{OUT})	1.8 V	
Minimum output voltage (V_{MIN})	1.59 V	
Maximum output voltage (V_{MAX})	1.85 V	
Number of phases	8	
Switching frequency	900 kHz	
Load step	60 A-430 A, 1,000 A/µs, 1 kHz-1 MHz	
Load line	0.5 mΩ	
L_M/L_{BUCK}	70 nH	120 nH
L_C	N/A	100 nH
C_{BULK} (polymer)	5 × 470 µF	0 × 470 µF
Multilayer ceramic capacitors (MLCCs)	80 × 22 µF, 0402	80 × 22 µF, 0402
	45 × 47 µF, 0805	56 × 47 µF, 0603
	15 × 100 µF, 0805	0 × 100 µF, 0805
	8 × 0.1 µF, 0402	8 × 0.1 µF, 0402
Peak power efficiency (η_{PEAK})	94.0%	93.9%
Full load efficiency (η_{Full})	88.1%	88.1%
V_{MIN} measured (worst case)	1.600 V (+10-mV margin), dominated by R_{LL}	1.600 V (+10-mV margin), dominated by R_{LL}
V_{MAX} measured (worst case)	1.846 V (+4-mV margin)	1.839 V (+11-mV margin)
Total output capacitance (C_{OUT})	7.7 mF	4.4 mF

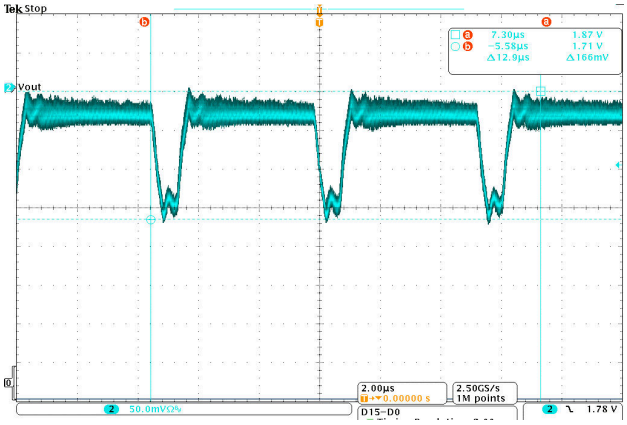
Table 5. *Design parameters.*



V_{MAX} = 1.846 V D = 20%

f_{SW} = 330 kHz

Figure 30. *Worst-case overshoot (multiphase buck converter).*



V_{MAX} = 1.839 V D = 10%

f_{SW} = 190 kHz

Figure 31. *Worst-case overshoot (TLVR).*

Summary

The TLVR topology is an evolution of the traditional multiphase buck converter design for high-phase-count, low-voltage nonisolated designs. It offers significant output capacitor savings and has become increasingly popular. In this paper, we introduced the concepts, operating principles, trade-offs, results from example designs, and practical considerations for TLVR designers.

Additional Resources

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