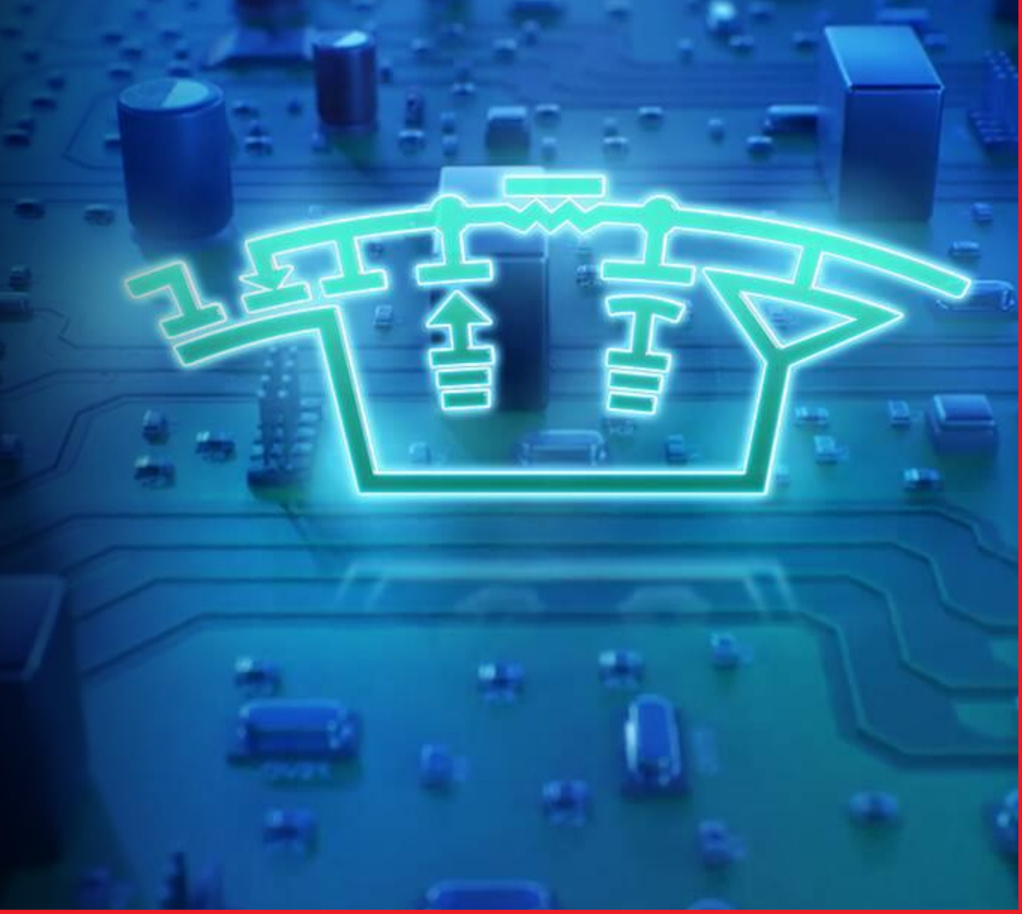
Texas Instruments

Power Supply Design Seminar

Introduction to the trans-inductor voltage regulator (TLVR)



Authors

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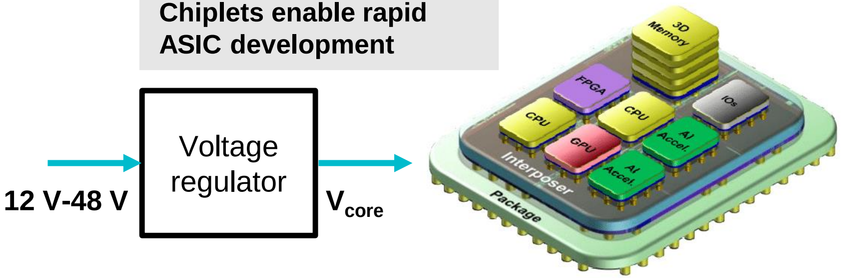
Agenda/overview

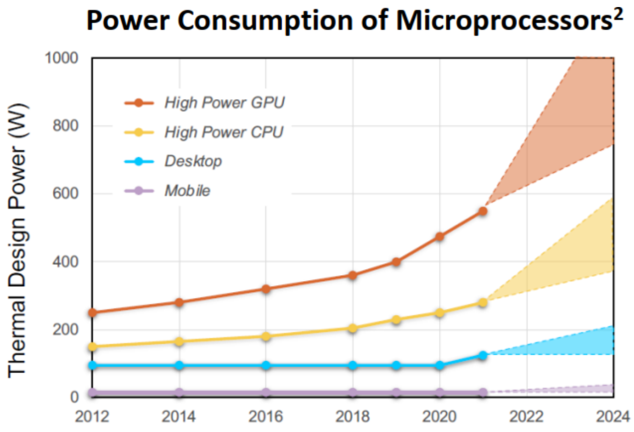
- Background and motivation
- Transinductor voltage regulator (TLVR) topology introduction
- Practical considerations
- Conclusion

Voltage regulator design challenges

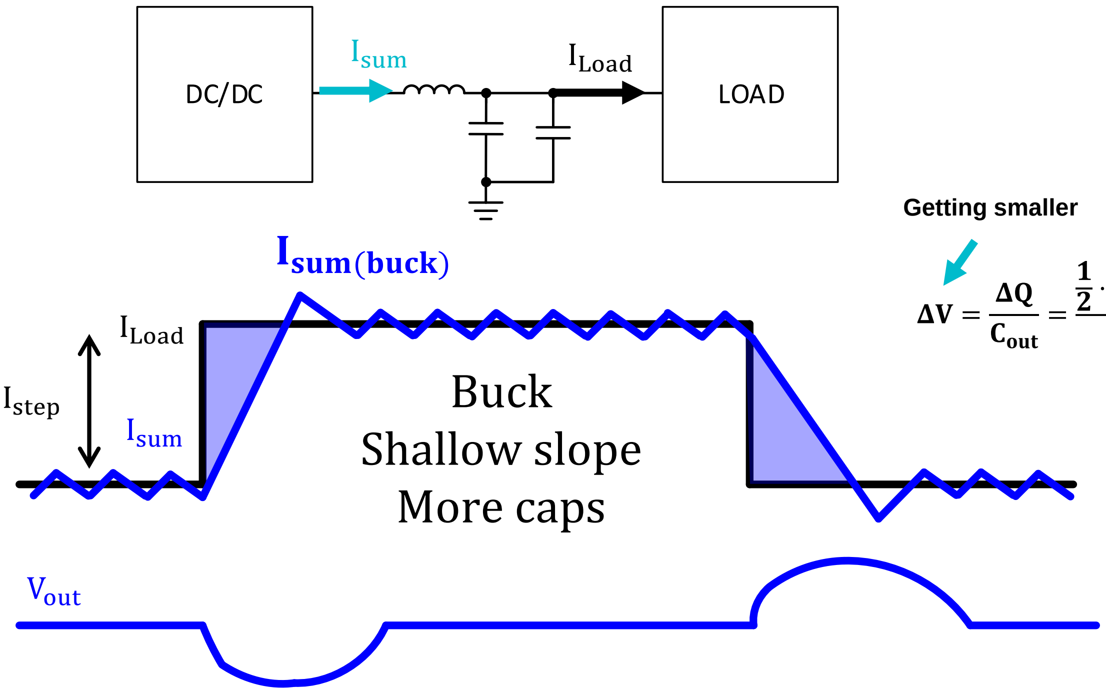
- **Silicon technology continues to shrink** (but this is slowing)
  3-nm digital → lower
- Application-specific integrated circuit (ASIC) **operating voltages remain** 0.7 V to 1.0 V (up to 1.8 V)
- High-core-count designs and chiplet revolution driving **rapid increase in operating currents**
  >1,000-A designs
- Extreme load transient requirements
  1,000 A/µs, ±3%

Chiplets enable rapid ASIC development





Motivation for TLVR: Improving transient response



Getting smaller

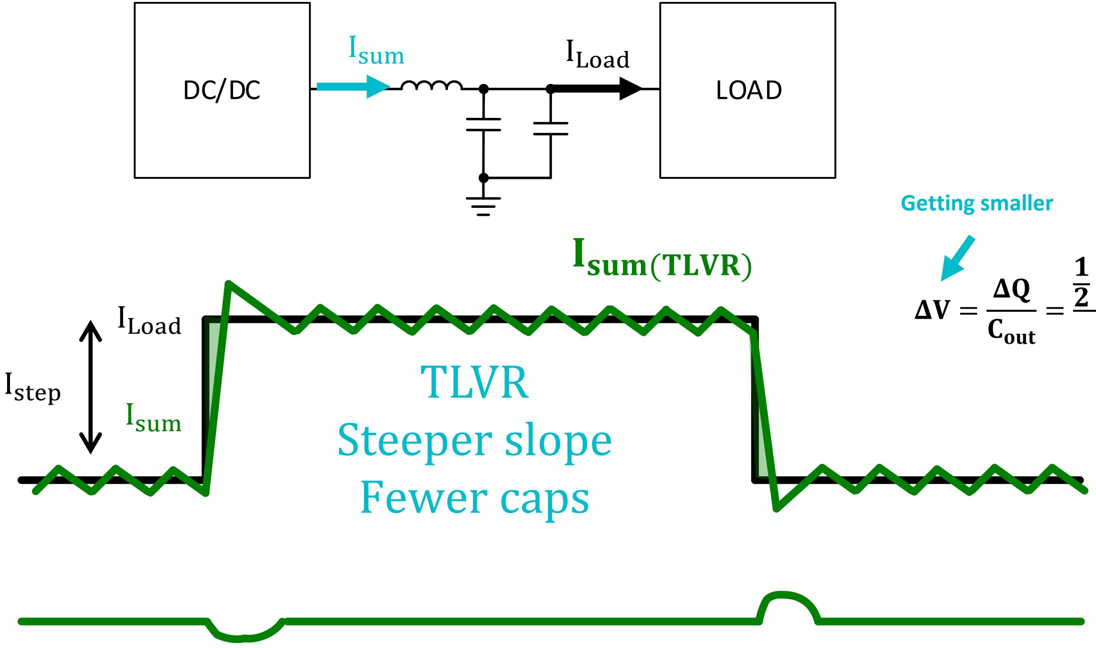
Getting bigger

$$\Delta V = \frac{\Delta Q}{C_{out}} = \frac{\frac{1}{2} \cdot t_{resp} \times I_{step}}{C_{out}} = \frac{\frac{1}{2} \times \frac{I_{step}^2}{\text{Slope}}}{C_{out}}$$

Getting expensive

Multiphase buck transient response

Motivation for TLVR: Improving transient response



TLVR buck transient response

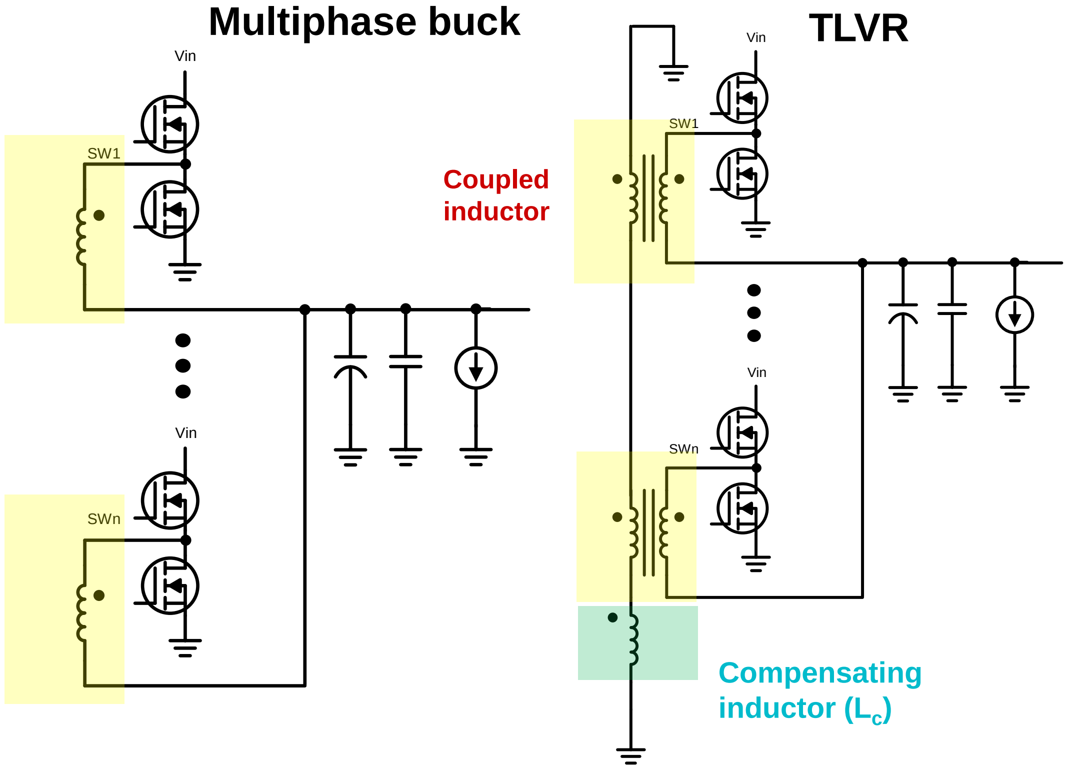
Getting smaller

Getting bigger

$$\Delta V = \frac{\Delta Q}{C_{out}} = \frac{\frac{1}{2} \times t_{resp} \times I_{step}}{C_{out}} = \frac{\frac{1}{2} \times \frac{I_{step}^2}{Slope}}{C_{out}}$$

Getting expensive

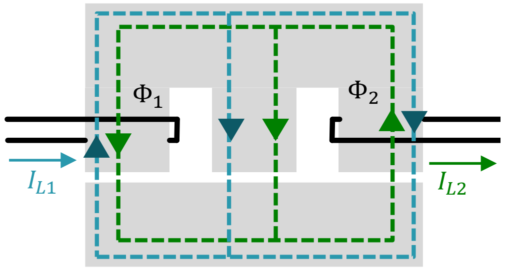
Buck converter vs. TLVR topology

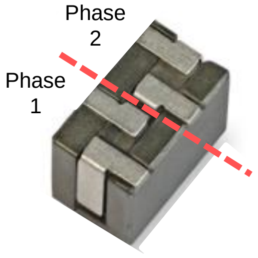


- **Buck-derived** topology optimized for fast transient response
- TLVR is a new twist on the coupled-inductor buck converter
- **When it makes sense:**
  - High phase count (>six phases)
  - High di/dt load transient
  - Moderate voltage ripple

Traditional coupled inductor

Traditional coupled inductor (two phase)

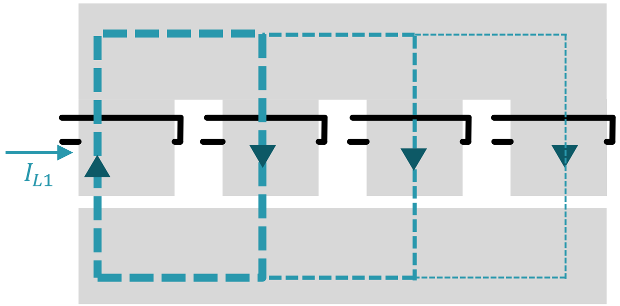




Two-phase coupled inductor
Source: Eaton

- Multiple windings share a single core
- Typical coupling coefficient: ≅0.5 to 0.7
- Higher power density
- Customized design for phase count/layouts

Difficult to extend to higher phases

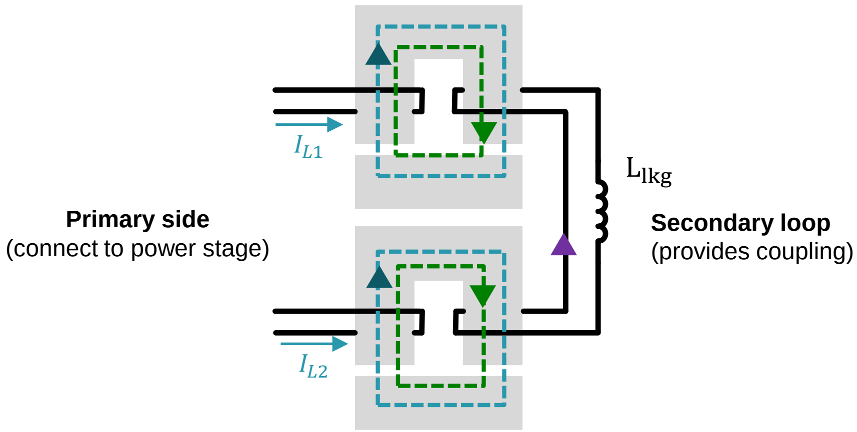


- **Challenge:** Symmetry is required for equal coupling among phases
- **Challenge:** Complex geometry required to maintain symmetry at higher phase counts

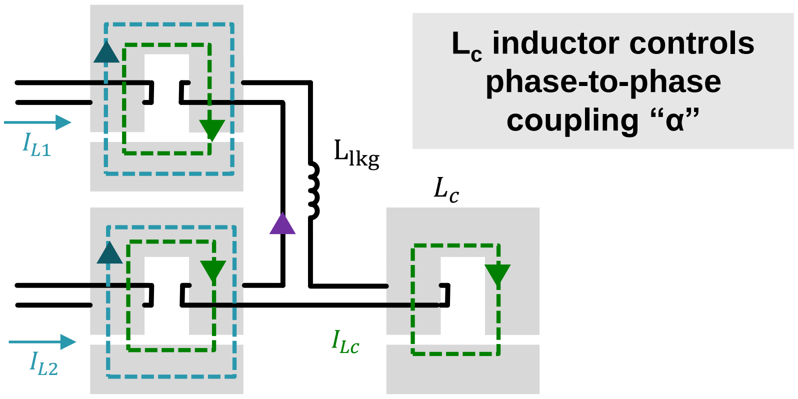
Coupling allows high steady state inductance (low ripple) and low transient inductance (fast transient)

Indirect-coupled inductor

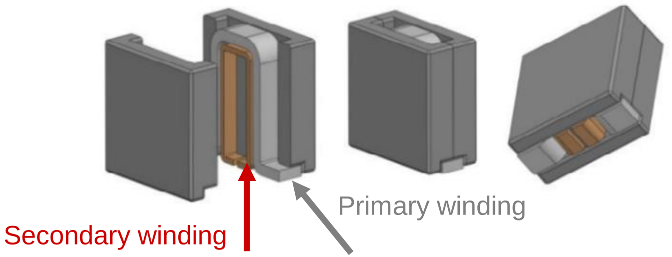
Indirect-coupled inductor (two phase)



TLVR: Indirect-coupling and compensating inductor (L_c)



- Phases are coupled symmetrically without a sharing core
- **Simple core geometry, scalable solution**
- **Challenging to control coupling**

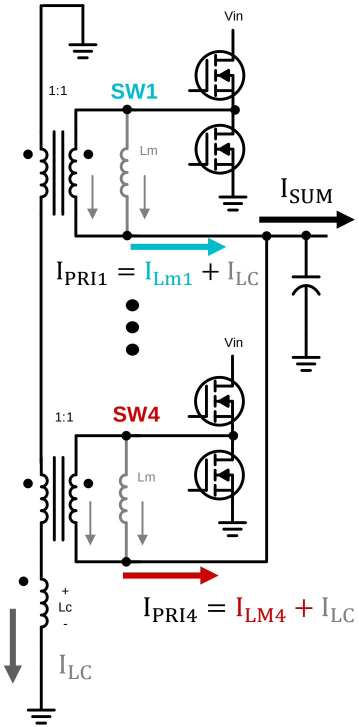


TLVR inductor construction

Source: Eaton

TLVR topology overview

TLVR operating principle: Steady state



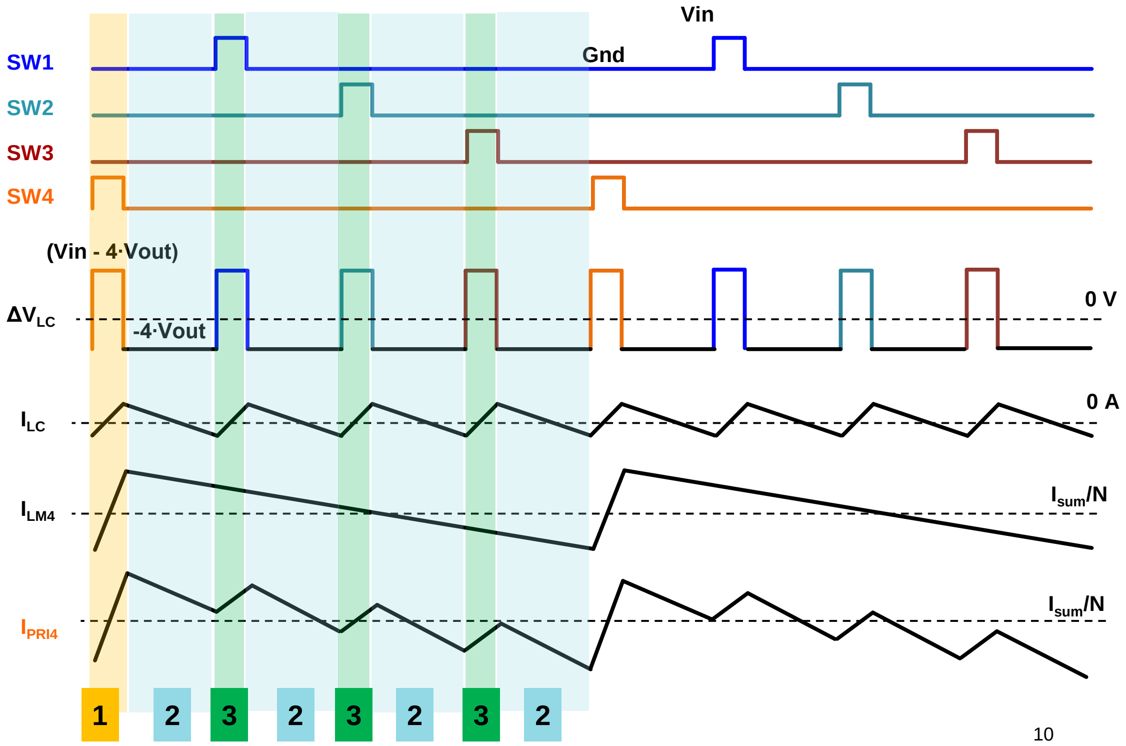
Phase current description (I_{PRI4})

1. This phase (SW4) is on; all others are off
   I_{LM4} increases
   I_{LC} increases

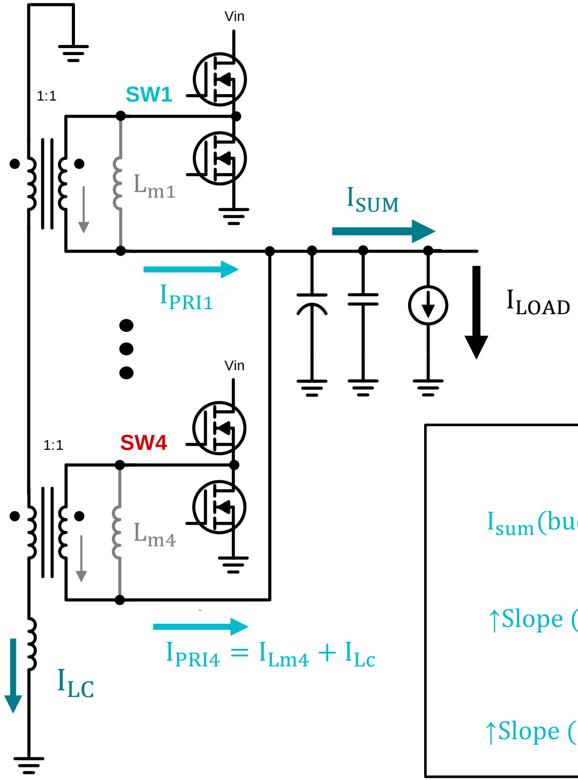
2. All phases are off
   I_{LM4} decreases
   I_{LC} decreases

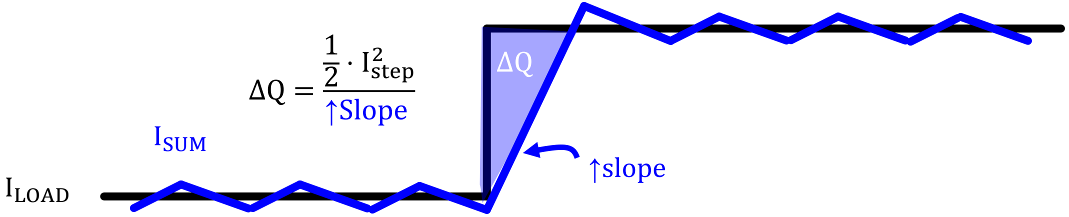
3. This phase (SW4) is off, but others are on
   I_{LM} decreases
   I_{LC} increases

TLVR steady-state operation (four-phase example, no overlap)



TLVR operating principle: Transient step-up





Controller **turns on multiple phases** in response.

N_{ON} phases are on, N_{OFF} phases are off

Multiphase buck

$$I_{sum}(buck) = I_{L1} + I_{L2} + \cdots$$

$$\uparrow Slope\ (buck) = \frac{\Delta V_{L1}}{L} + \frac{\Delta V_{L2}}{L} + \cdots$$

$$\uparrow Slope\ (buck) \approx N_{on}\left(\frac{V_{in} - V_{out}}{L}\right) - N_{off}\left(\frac{V_{out}}{L}\right)$$

TLVR

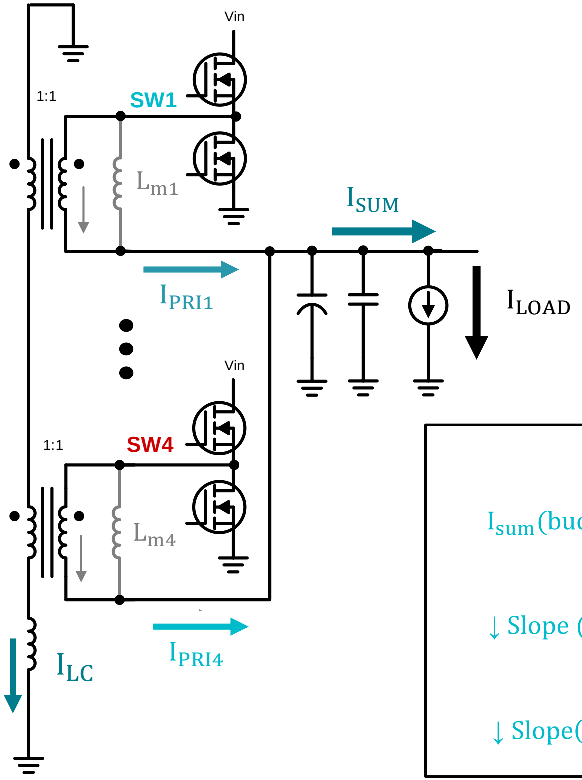
$$I_{sum}(TLVR) = I_{pri1} + I_{pri2} + \cdots$$

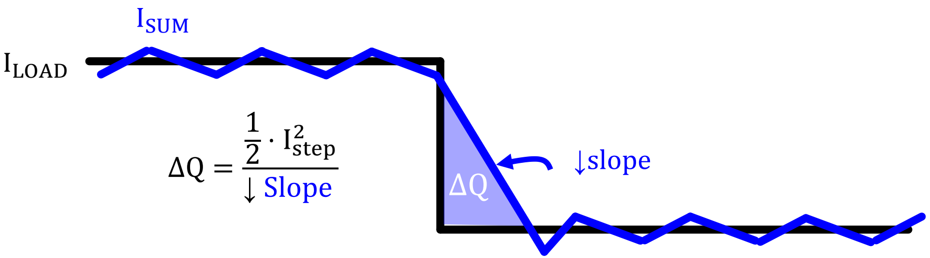
$$I_{sum}(TLVR) = (I_{Lm1} + \mathbf{I_{Lc}}) + (I_{Lm2} + \mathbf{I_{Lc}}) + \cdots$$

$$\uparrow Slope\ (TLVR) = \left(\frac{\Delta V_{L1}}{L_m} + \frac{\mathbf{\Delta V_{Lc}}}{\mathbf{L_c}}\right) + \left(\frac{\Delta V_{L2}}{L_m} + \frac{\mathbf{\Delta V_{Lc}}}{\mathbf{L_c}}\right) + \cdots$$

$$\uparrow Slope\ (TLVR) \approx \uparrow Slope(buck) + \mathbf{N_{total}}\left[\frac{\mathbf{N_{on} \cdot V_{IN} - N_{total} \times V_{OUT}}}{\mathbf{L_c}}\right]$$

TLVR operating principle: Transient step-down





$$\Delta Q = \frac{\frac{1}{2} \cdot I_{step}^2}{\downarrow \text{Slope}}$$

Controller **turns off all phases** in response

N_{TOTAL} phases are off

Multiphase buck

$$I_{sum}(\text{buck}) = I_{L1} + I_{L2} + \cdots$$

$$\downarrow \text{Slope (buck)} = \frac{\Delta V_{L1}}{L} + \frac{\Delta V_{L2}}{L} + \cdots$$

$$\downarrow \text{Slope(buck)} \approx -N_{total}\left(\frac{V_{out}}{L}\right)$$

TLVR

$$I_{sum}(\text{TLVR}) = I_{pri1} + I_{pri2} + \cdots$$

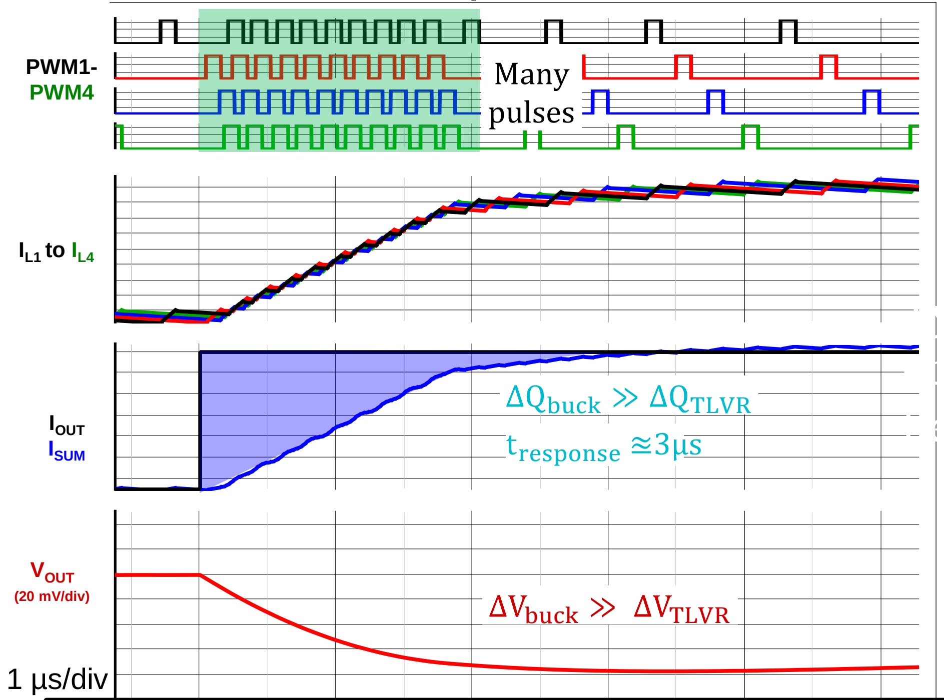
$$I_{sum}(\text{TLVR}) = (I_{Lm1} + \mathbf{I_{Lc}}) + (I_{Lm2} + \mathbf{I_{Lc}}) + \cdots$$

$$\downarrow \text{Slope (TLVR)} = \left(\frac{\Delta V_{L1}}{L_m} + \frac{\mathbf{\Delta V_{Lc}}}{\mathbf{L_c}}\right) + \left(\frac{\Delta V_{L2}}{L_m} + \frac{\mathbf{\Delta V_{Lc}}}{\mathbf{L_c}}\right) + \cdots$$

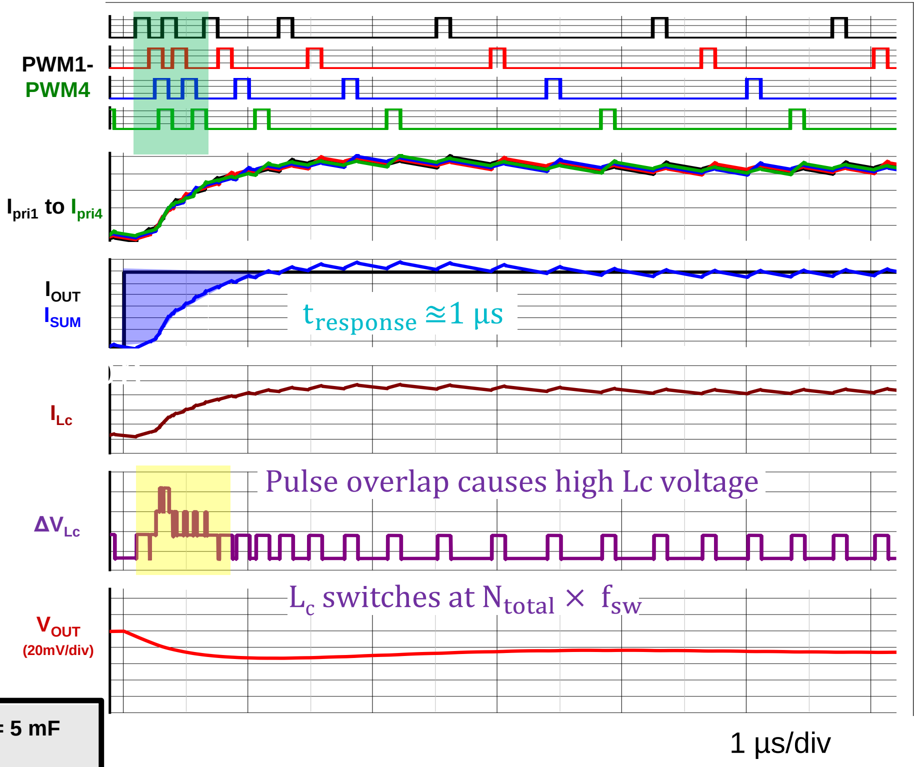
$$\downarrow \text{Slope (TLVR)} \approx \downarrow \text{Slope(buck)} - \mathbf{N_{total}}\left[\frac{\mathbf{N_{total} \times V_{OUT}}}{\mathbf{L_c}}\right]$$

Side-by-side comparison: Load step-up

Multiphase buck



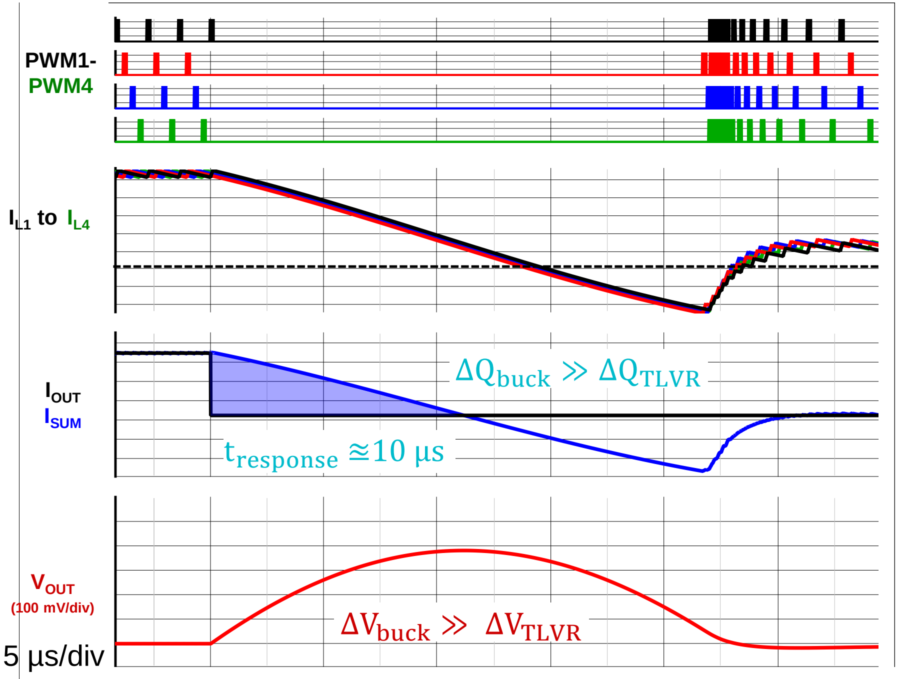
TLVR



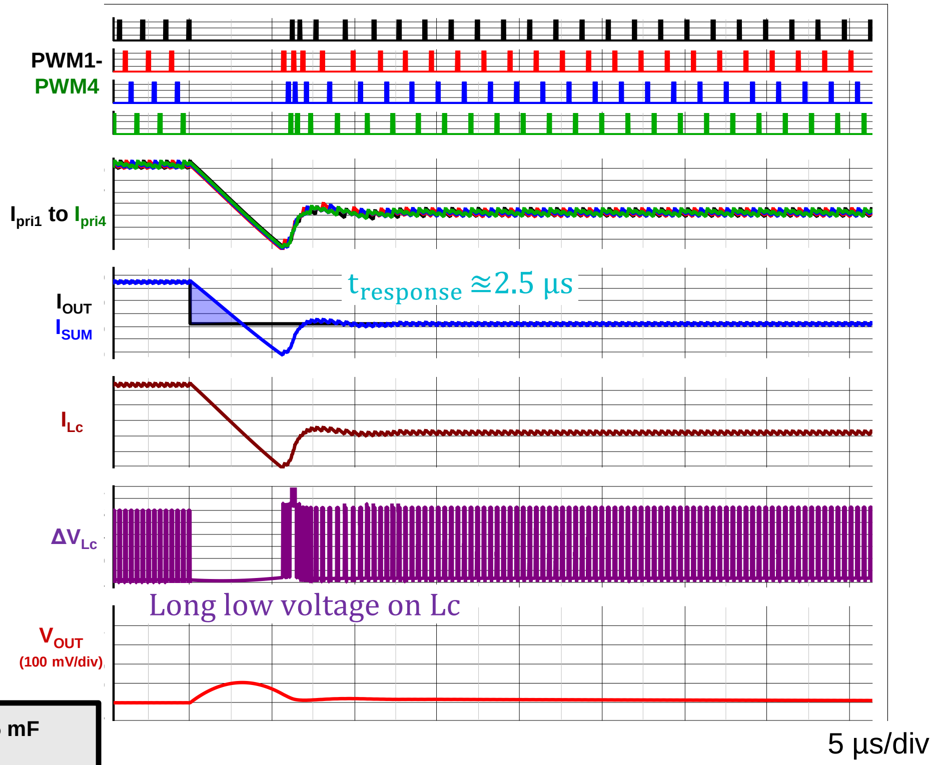
- V_{IN} = 12 V
- V_{OUT} = 0.8 V
- F_{sw} = 600 kHz, four phases
- I_{OUT} = 25 A-325 A, instantaneous
- Buck: L buck = 150 nH
- TLVR: L_m = 150 nH, L_c = 180 nH
- C_{OUT} = 5 mF

Side-by-side comparison: Load step-down

Multiphase buck



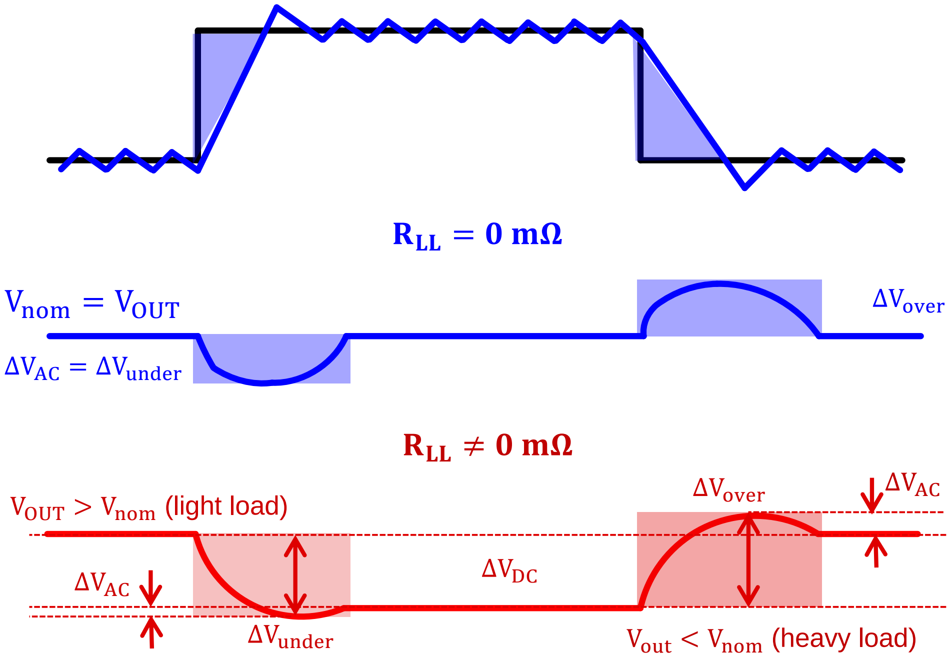
TLVR



- V_{IN} = 12 V
- V_{OUT} = 0.8 V
- F_{sw} = 600 kHz, four phases
- I_{OUT} = 25 A-325 A, instantaneous
- Buck: L_buck = 150 nH
- TLVR: L_m = 150 nH, L_c = 180 nH
- C_{OUT} = 5 mF

DC load line further reduces output capacitance

DC load-line (DCLL) behavior is **identical** between buck and TLVR designs



$$R_{DCLL} = \frac{\Delta V_{DC}}{\Delta I_{step}}$$

Capacitor savings

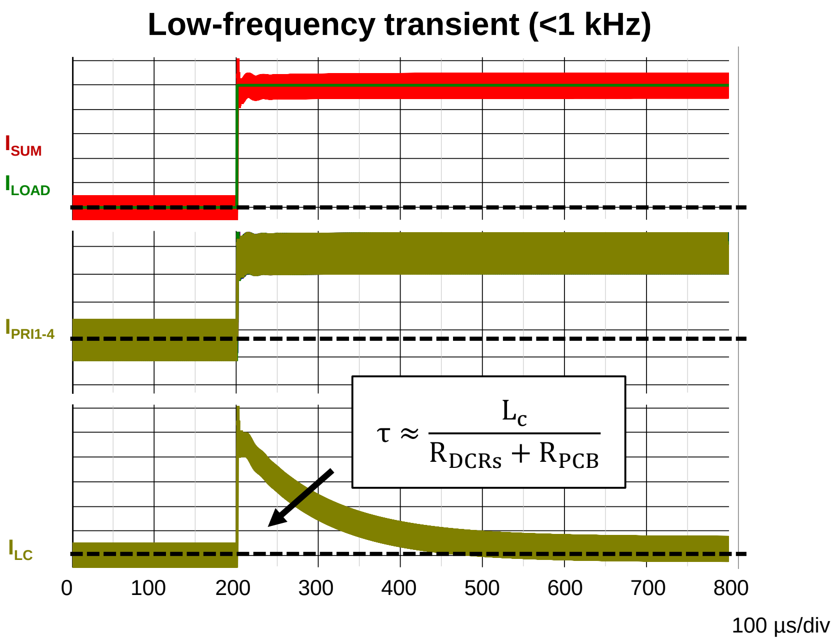
$$C_{out(min,\, step\ up)} = \frac{\Delta Q_{under}}{\Delta V_{under}} = \frac{\Delta Q_{under}}{\Delta V_{ac} + R_{LL} \times I_{step}}$$

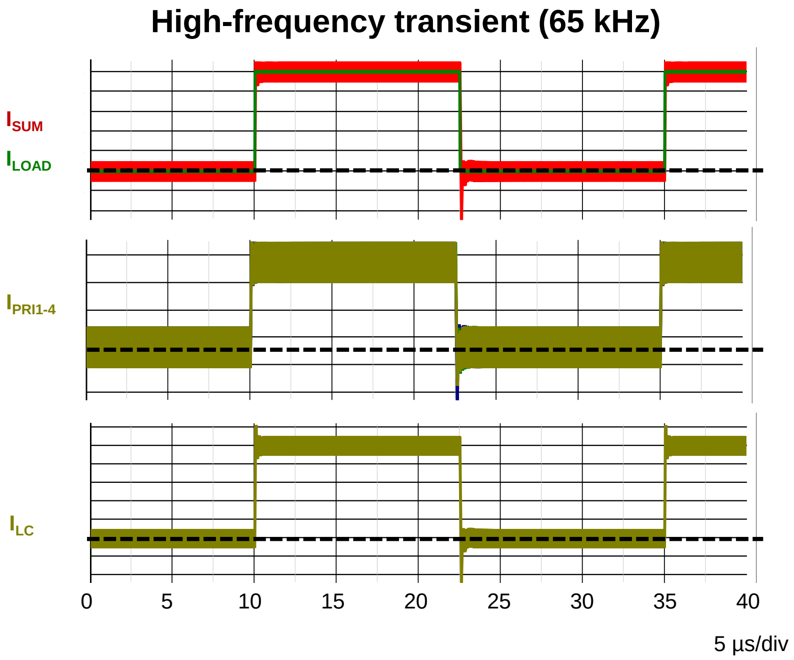
$$C_{out(min,\, step\ down)} = \frac{\Delta Q_{over}}{\Delta V_{over}} = \frac{\Delta Q_{over}}{\Delta V_{ac} + R_{LL} \times I_{step}}$$

Reduced output power

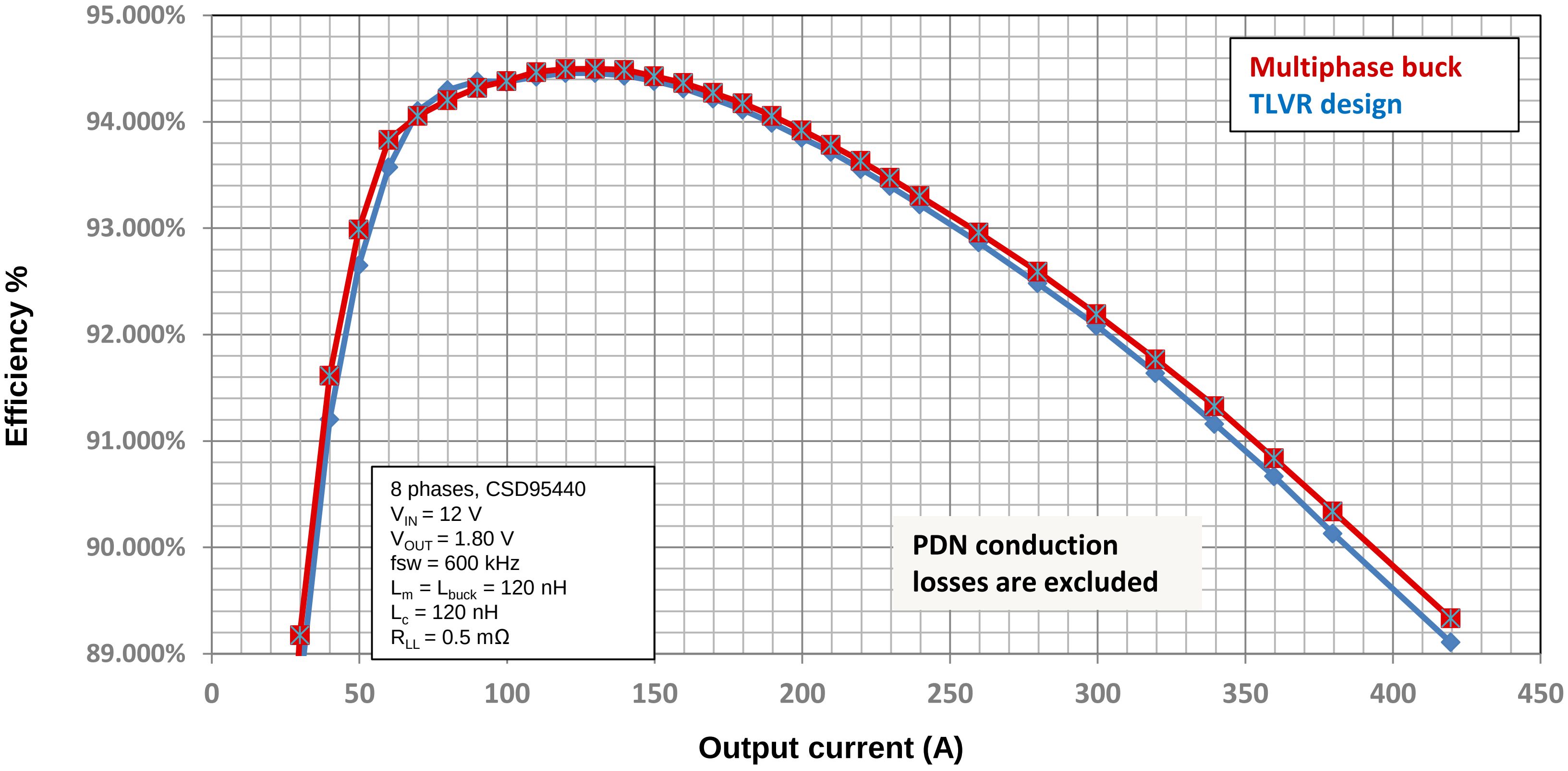
$$P_{out} = I_{out} \times (V_{out} - R_{LL} \times I_{out})$$

L_c as an AC inductor – I_{LC} during a transient

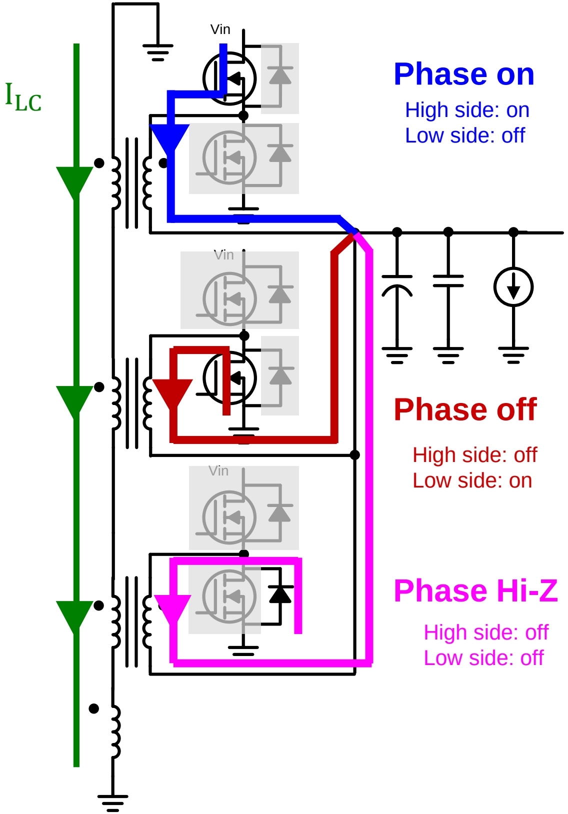




VR vs. TLVR efficiency comparison ($L_{BUCK} = L_M = L_C$)



Dynamic phase shedding

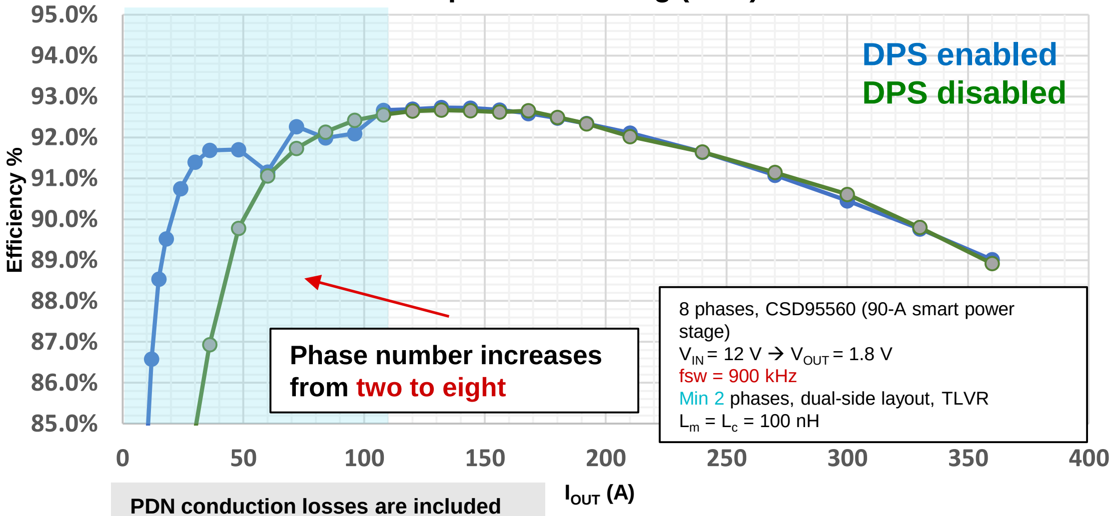


0 when DPS is off

$$\Delta V_{Lc} = N_{on} \times (V_{IN} - V_{OUT}) + N_{off} \times (-V_{OUT}) + N_{HiZ} \times (V_{diode})$$

$$P_{cond,HiZ} \approx I_{rms(L_c)} \times V_{diode} \qquad P_{cond,HiZ} \ll P_{switching}$$

Efficiency comparison (including power delivery network [PDN]) vs. dynamic phase shedding (DPS)

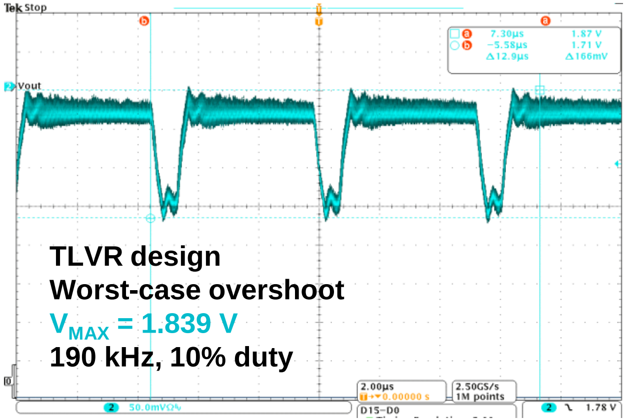


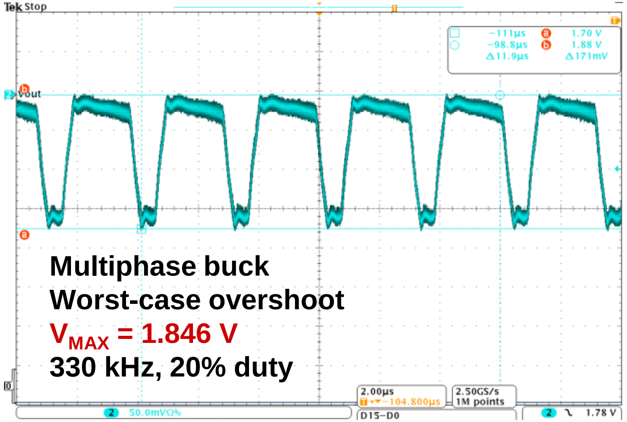
PDN conduction losses are included

Example side-by-side design

Parameter	TLVR	Multiphase buck
Controller/SPS	TPS53689, CSD95440	
V_{IN}	12 V	
V_{OUT}	1.8 V	
Number of phases	8 phases	
Switching frequency	900 kHz	
Load step	60 A-430 A, 1,000 A/µs, 1 kHz-1 MHz	
Load line	0.5 mΩ	
L_m/L_{buck}	150 nH	70 nH
L_c	100 nH	–
C_{bulk} (polymer)	0 × 470 µF	5 × 470 µF
Multilayer ceramic capacitors	80 × 22 µF 0402	80 × 22 µF 0402
	56 × 47 µF 0603	45 × 47 µF 0805
	0 × 100 µF 0805	15 × 100 µF 0805
	8 × 0.1 µF 0402	8 × 0.1 µF 0402
Total C_{out}	4.4 mF	7.7 mF

More transient margin with 45% reduction
in output capacitance required





Practical considerations

L_c inductor selection

- Typically select L_c between L_m and $1.25 \times L_m$
- Minimal root-mean-square current (RMS) required

$$I_{rms(L_c)} \approxeq \frac{\Delta I_{Lc}}{\sqrt{12}}$$

- High saturation current required

$$I_{sat} \gg t_{resp} \times \left[\frac{N_{on(step)} \times V_{IN} - N_{total} \times V_{OUT}}{L_c}\right]$$

- Voltage across L_c can be $\gg V_{IN}$

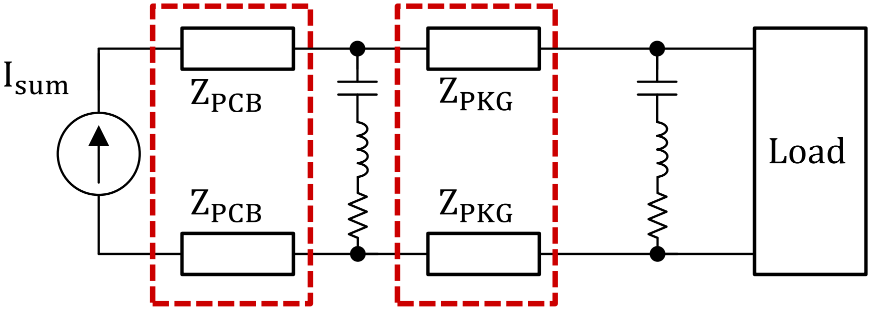
$$V_{LC(max)} = N_{on(step)} \times V_{IN} - N_{total} \times V_{OUT}$$

Example L_c selection

Parameter	Value
V_{IN}	12 V
V_{OUT}	0.8 V
F_{sw}	600 kHz
N_{total}	8 phases
L_m	150 nH
L_c	180 nH
Load transient	50-500 A, 1,000 A/µs
ΔI_{Lc}	5.0 A
F_{LC}	4.8 MHz
$I_{RMS(Lc)}$	2.8 A
Margin for I_{SAT}	25%
$I_{SAT(min)}$	75 A
$\Delta V_{Lc(max)}$	30 V ($N_{OVERLAP}$ = 3)

Output-ripple cancellation

Output-voltage ripple (simple model)

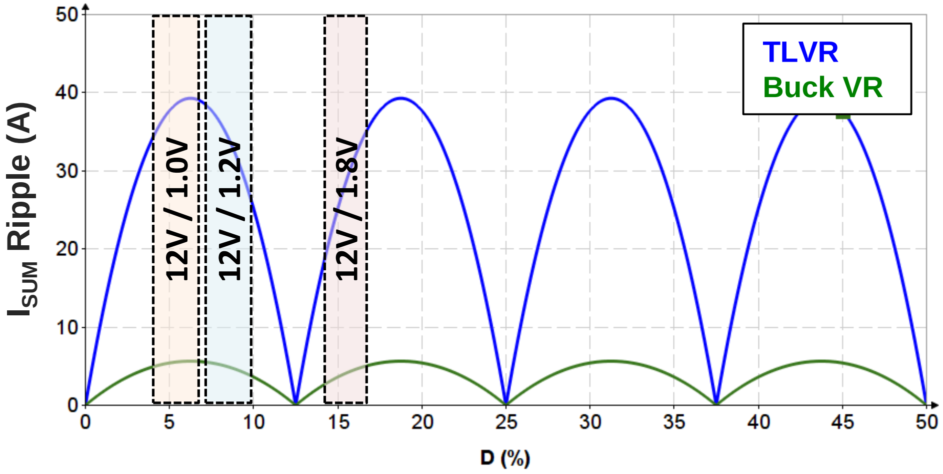


Same L_c current gets added at every phase-shift offset

$$I_{sum} = (I_{Lm1} + I_{Lc}) + (I_{Lm2} + I_{Lc}) + \cdots$$

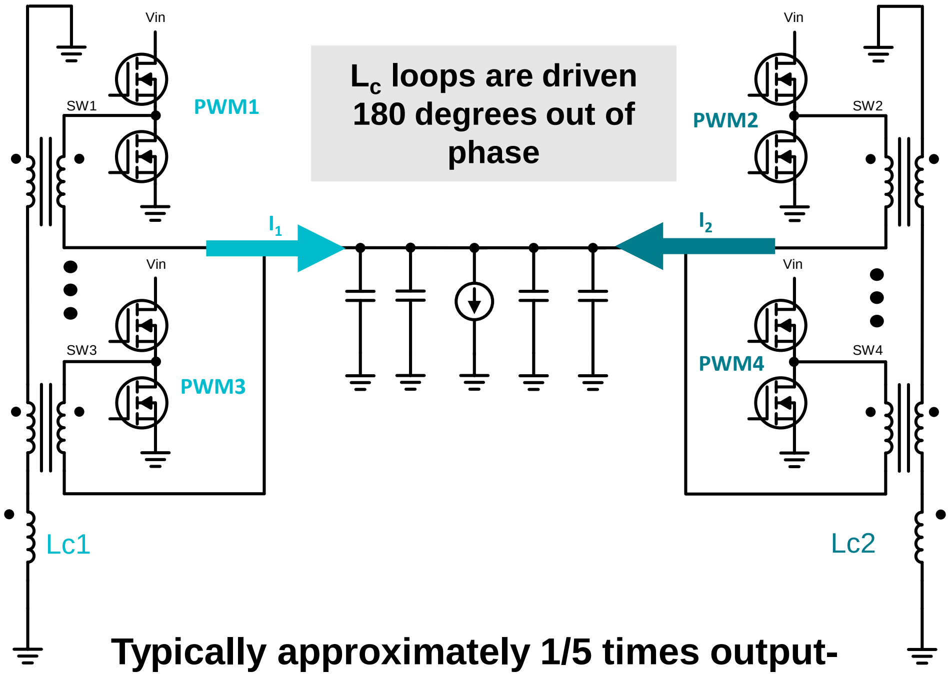
$0 \times \frac{360°}{N}$ phase shift $\quad 1 \times \frac{360°}{N}$ phase shift

Example:
TLVR vs. multiphase buck I_{OUT} ripple vs. duty cycle



V_{IN} = 12 V, F_s = 700 kHz, L_m = 150 nH, L_c = 120 nH, $L_{VR} = L_{eq}$ = 125 nH, eight phases

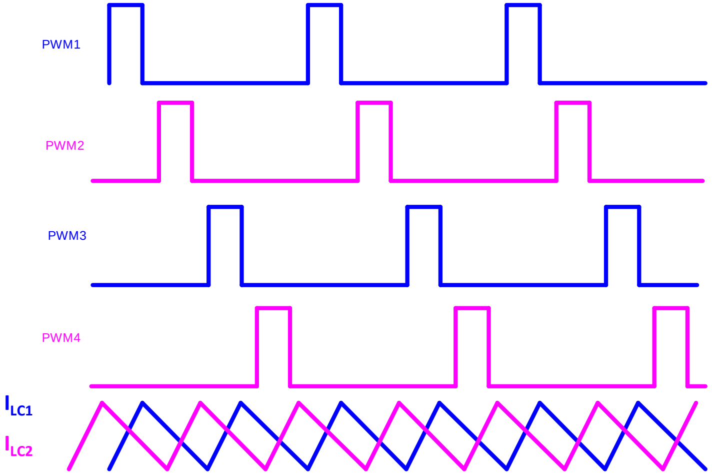
Reduced ripple voltage: Interleaved TLVR



L_c loops are driven 180 degrees out of phase

Typically approximately 1/5 times output-voltage ripple for 12-V → 1-V TLVR design

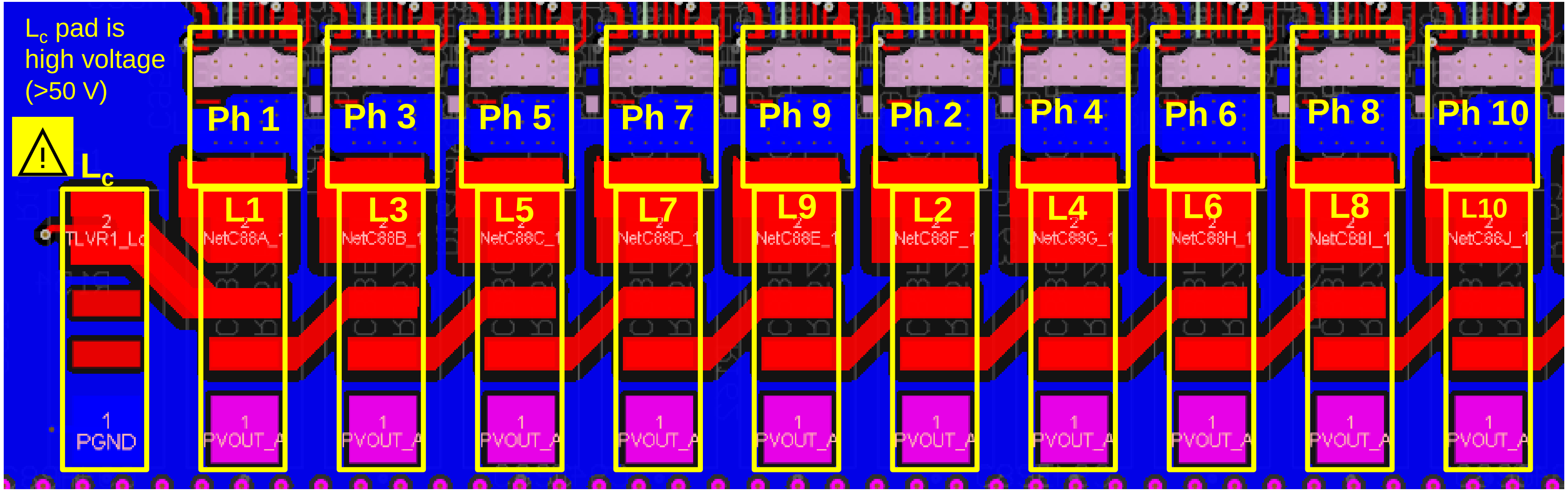
- For high-phase-count (>12 phase) designs, creating two (or more) L_c loops achieves interleaving
- May also be advantageous for layout and electromagnetic interference (EMI) concerns (reduced L_c frequency, reduced maximum L_c voltage)



Typical power-stage layout

- Interleaving phase fire order reduces crosstalk and reduces input capacitor stress

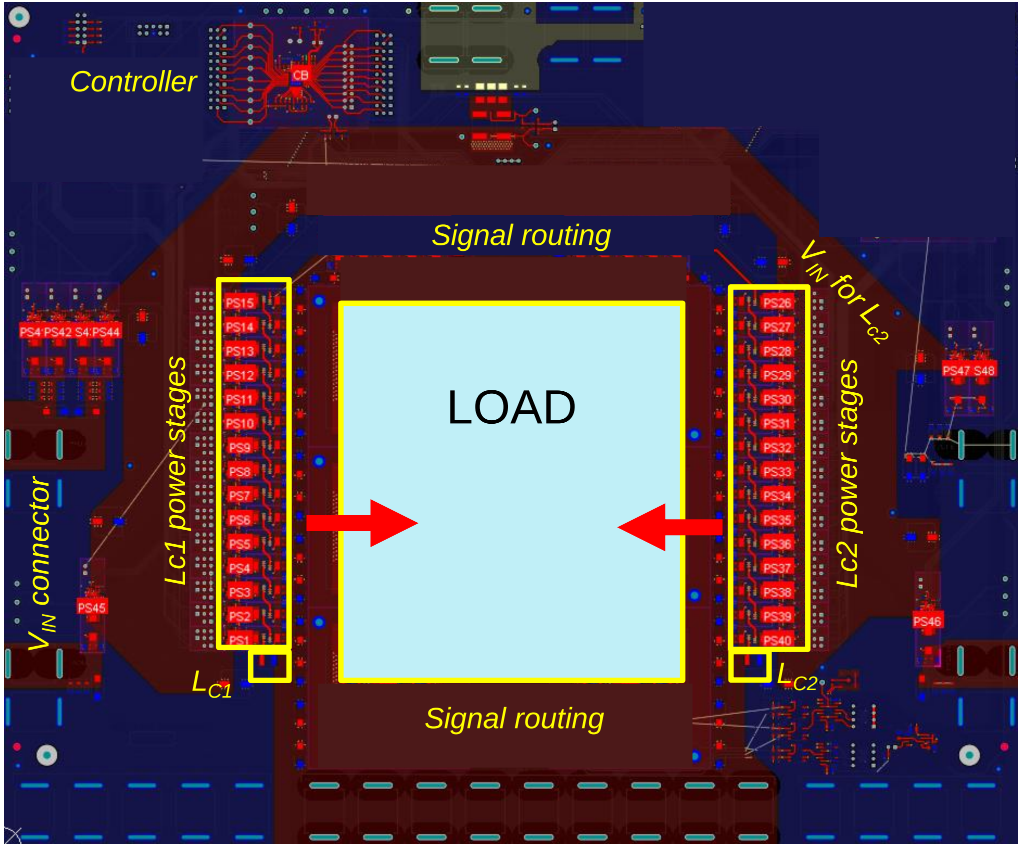
- L_c current still carries high current in a transient
- Recommend ≅50 mils



Option for reduced EMI 1/2 L_c on each end

1/2 L_c

Printed circuit board layout: Multiside power delivery



Example:

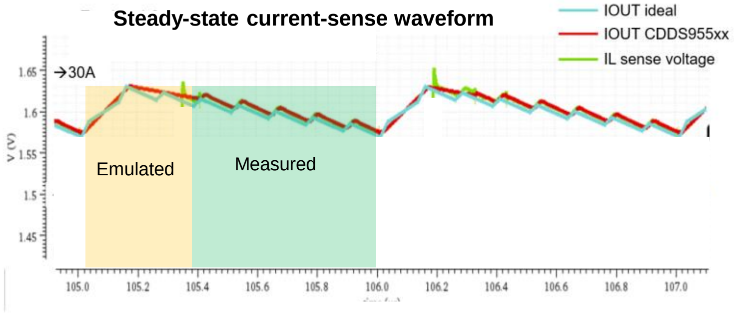
- 32-phase design
- Two L_c interleaved design

Recommendations:

- Symmetrical power train and L_c layout
- Decoupling and current-resistance (IR) drop on input traces
- PWM pin trace capacitance
  - Controller PWM drive strength
- Current-sense trace capacitance
  - Low-pass filter effect for current monitor (Imon) signals

TLVR-optimized controllers and power stages

TLVR-optimized power stages

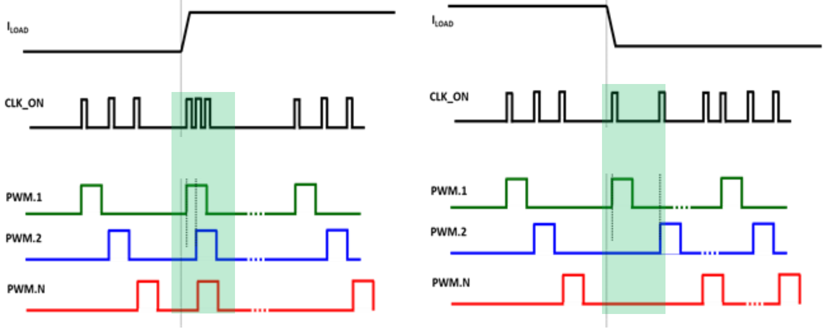


High bandwidth, real current information reporting

Part number	Current rating	Package/features
CSD95440	80-A peak, 40 A_{RMS}	5 mm × 6 mm (voltage Imon)
CSD95510	90-A peak, 50 A_{RMS}	4 mm × 6 mm (voltage Imon)
CSD95560	90-A peak, 50 A_{RMS}	4 mm × 6 mm (current Imon)
CSD95520	60-A peak, 30 A_{RMS}	4 mm × 5 mm (voltage Imon)
CSD95570	60-A peak, 30 A_{RMS}	4 mm × 5 mm (current Imon)

TLVR-optimized controllers

PWM-based L_c current emulation (patent pending)



Load transient detection based on PWM timing

Part number	Phases	Package/features
TPS53685	8	5 mm × 5 mm AMD interface
TPS536C5	12	6 mm × 6 mm AMD interface
TPS53689T	8	5 mm × 5 mm Intel interface
TPS536C9T	12	6 mm × 6 mm Intel interface

Conclusion

Summary

- Introduced the TLVR topology
  - Buck-derived topology similar to coupled inductors for high-phase-count designs
  - Better modularity and reuse for TLVR, since inductors do not share a core
  - Significant output capacitor savings given coupled-inductor behavior
- Practical considerations for TLVR designs
  - TLVR designs typically have higher ripple current and voltage vs. buck
  - Interleaving for high-phase-count designs
  - Printed circuit board layout for TLVR designs is similar to buck, with L_c loop added
- TLVR-optimized components
  - High-bandwidth and system-level optimizations needed to optimize for TLVR designs

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