

Power Supply Design Seminar

GaN-optimized transition-mode power factor correction

Author

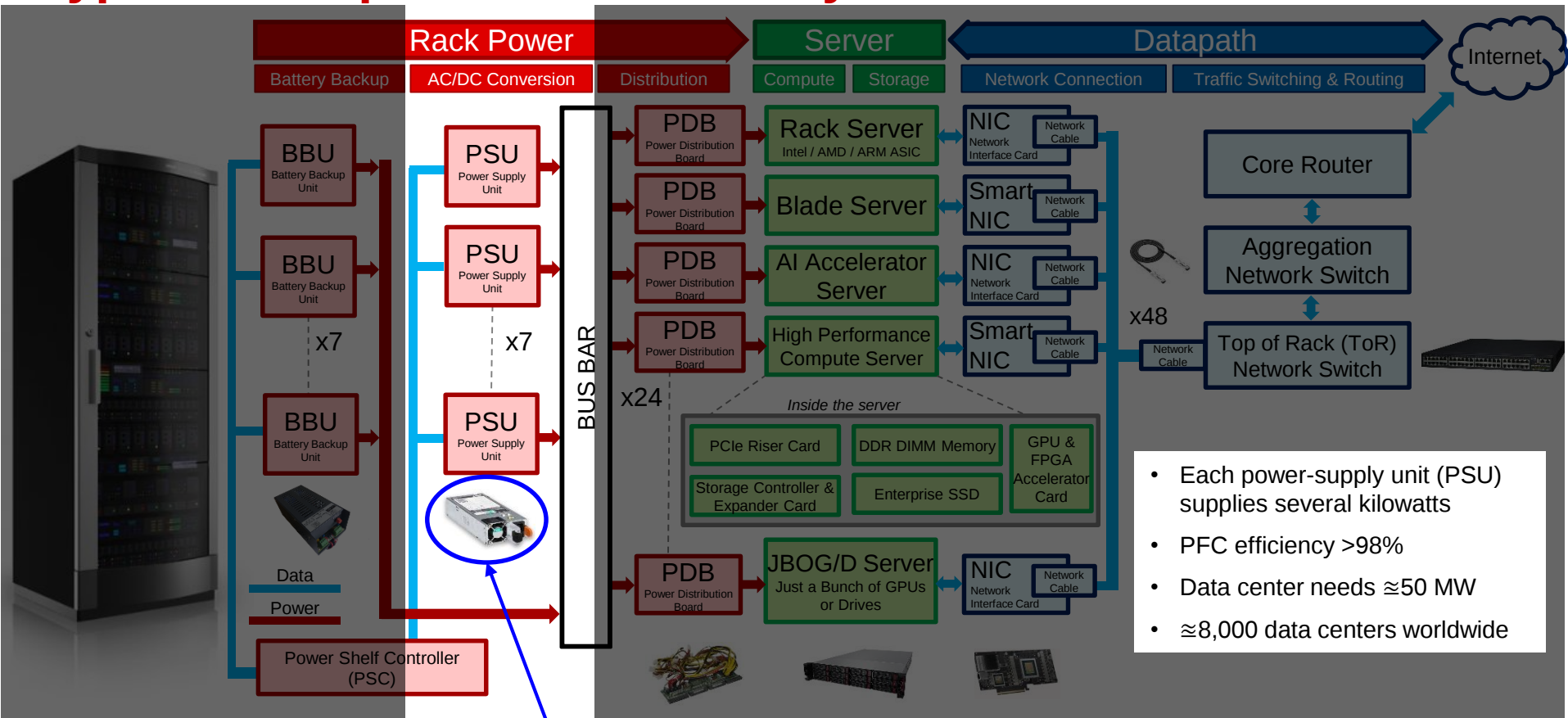
Brent McDonald



Agenda

- Applications
- Boost converter
 - Topology review
 - Conduction modes
- Control methods
 - Constant on-time
 - Zero current detection (ZCD)
 - Zero voltage detection (ZVD)
- Experimental results
- Conclusions

Typical enterprise data center system



Power factor correction (PFC) circuit

Totem-pole PFC – using one boost converter for PFC

Positive half cycle

Negative half cycle

Control field-effect transistor (FET) “D”

- Can you control the input current with one boost converter?
- Yes, if you add the ability to reconfigure the circuit during each half cycle

Rectifier “1-D”

Totem-pole PFC

Strengths

- Highest efficiency
- Minimizes conduction loss

Weaknesses

- Control complexity
- Usually requires wide band-gap switches
- Current sensing
- Common-mode electromagnetic interference (EMI)

Positive half cycle

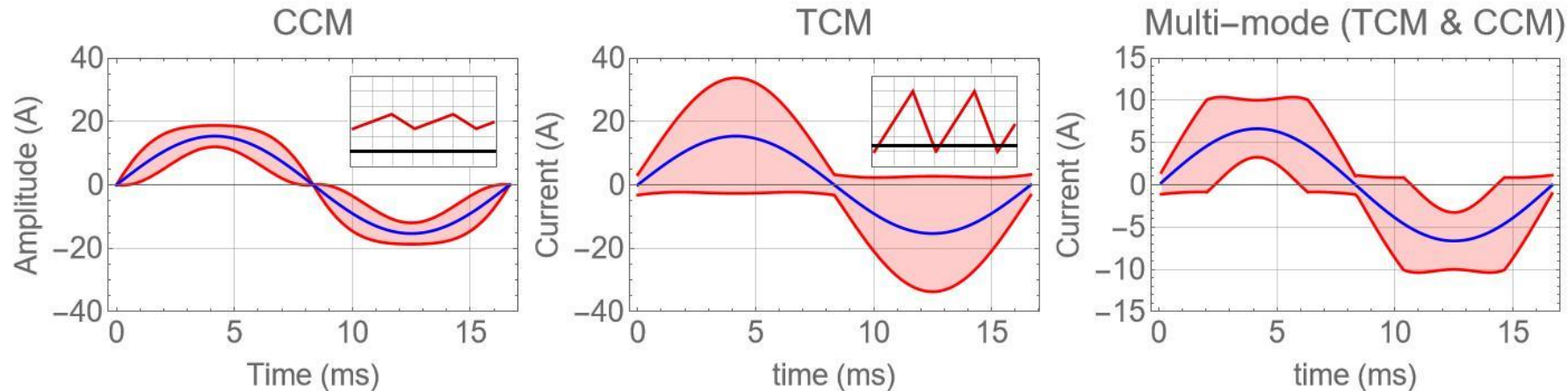
Negative half cycle

Control FET “D”

Synchronous
rectifier “1-D”

[CCM totem-pole PFC paper](#)

PFC conduction modes



— Ripple Current Envelope — Average Current

Continuous conduction mode (CCM)

- Hard switching and reverse recovery
- Lower conduction loss
- Small ripple current
- Simple control

Transition conduction mode (TCM)

- Zero voltage switching (ZVS)
- Higher conduction loss
- Large ripple
- Complex control

Multimode

- Combination of CCM/TCM
- Attempts to get benefits of each
- Complex control

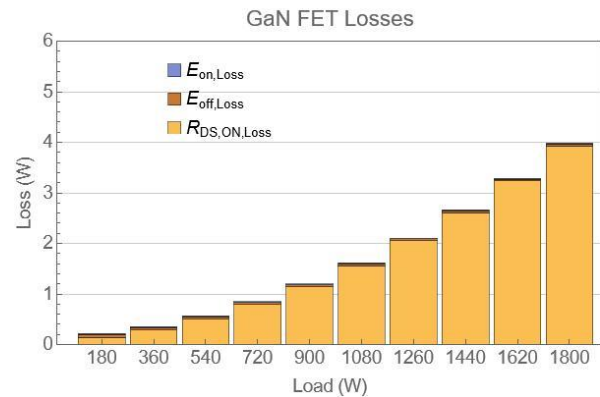
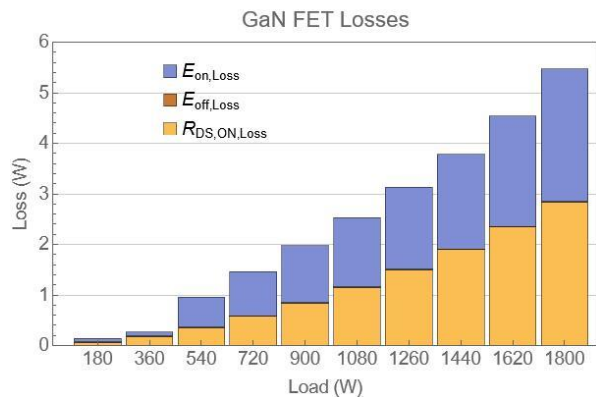
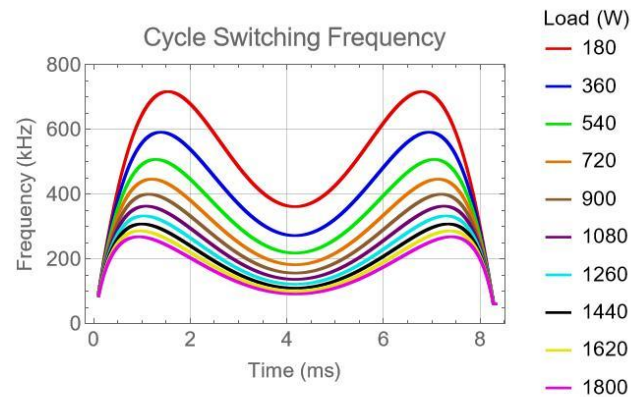
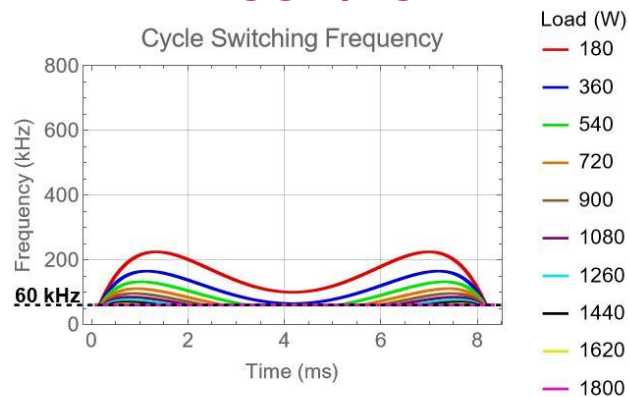
$\langle I_{L_g}(t) \rangle_{T_s}$ denotes the current in L_g averaged over each switching cycle

Conduction-mode impact on FET losses

CCM/TCM

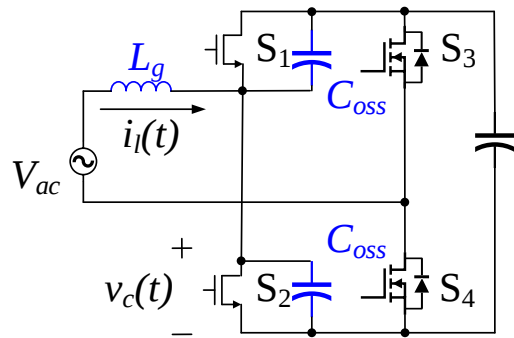
TCM

Topology	CCM/TCM	TCM
Inductor	150 μ H	25 μ H
f_s range	60 kHz-250 kHz	75 kHz-750 kHz
FET loss	High	Low
Inductor volume	Big	Small
EMI filter size	Small	Big

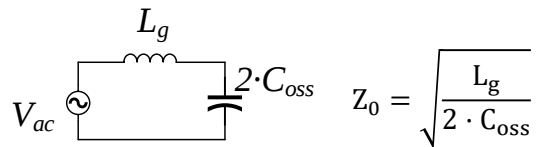


Control constraints

TCM converter



ZVS equivalent circuit



$$i_l(t) = 2 \cdot C_{oss} \cdot \frac{dv_c(t)}{dt}$$

$$v_{ac}(t) - v_c(t) = L_g \frac{di_l(t)}{dt}$$

- PFC requirements

- Condition No. 1: ZVS

- S_1 achieves ZVS if $v_c(t) = v_{OUT}$ before turnon
 - S_2 achieves ZVS if $v_c(t) = 0$ before turnon

- Condition No. 2: low total harmonic distortion (THD)

- $v_{ac}(t) = \sqrt{2} \cdot v_{ac,rms} \cdot \sin(\omega \cdot t + \varphi)$
 - $\left\langle I_{L_g}(t) \right\rangle_{T_s} = \frac{v_{ac}(t)}{R_e}, R_e = \frac{v_{ac,rms}^2}{P_{out}}$

- Well-known solution to equivalent circuit

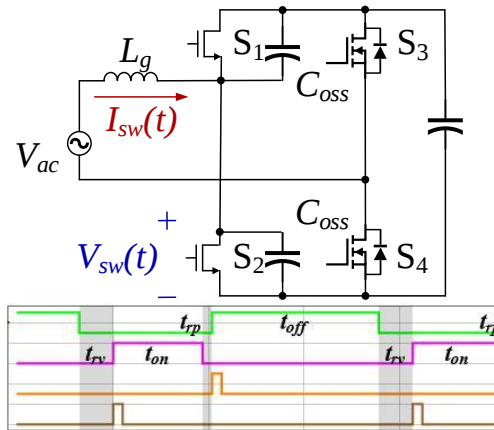
- $v_c(t) = i_l(t_0) \cdot Z_0 \cdot \sin(\omega_0 \cdot t) + (v_c(t_0) - v_{ac}(t_0)) \cdot \cos(\omega_0 \cdot t)$
 - $i_l(t) = \frac{(v_{ac}(t_0) - v_c(t_0))}{Z_0} \cdot \sin(\omega_0 \cdot t) + i_l(t_0) \cdot \cos(\omega_0 \cdot t)$

- Microcontroller solves for required timing

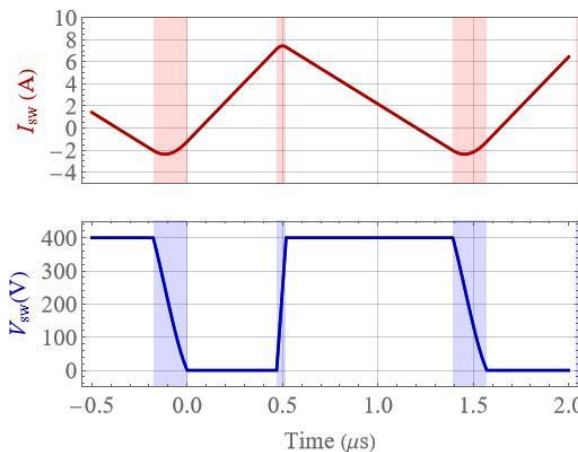
$\left\langle I_{L_g}(t) \right\rangle_{T_s}$ denotes the current in L_g averaged over each switching cycle

Control timing definitions

- Control variables
 - t_{on} – **on-time** of the **control FET**
 - t_{off} – **on-time** of the **synchronous rectifier (SR)**
 - t_{rp} – **dead time** between the **control FET turnoff** and **synchronous rectifier turnon**
 - t_{rv} – **dead time** between the **synchronous rectifier turnoff** and the **control FET turnon**
- Positive AC half cycle
 - S1 – synchronous rectifier
 - S2 – control FET
- Negative AC half cycle
 - S1 – control FET
 - S2 – synchronous rectifier



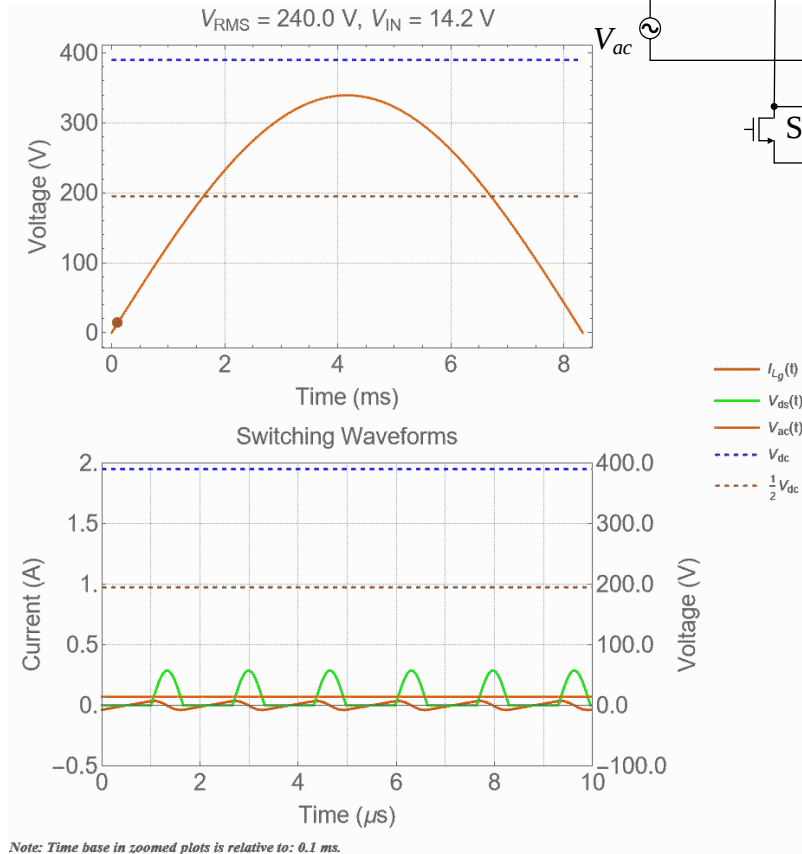
$V_{hs,g}$, High Side Gate
 $V_{ls,g}$, Low Side Gate
 $V_{hs,zvd}$, High Side ZVD
 $V_{ls,zvd}$, Low Side ZVD



Transition-mode control – COT

- Constant on-time (COT) control
 - $\left\langle I_{L_g}(t) \right\rangle_{T_s} = \frac{V_{ac}(t)}{2 \cdot L_g} t_{on}$
- Operates on the discontinuous-conduction-mode (DCM)/CCM boundary
- Large switching frequency variation
- The inductor current will go negative every cycle
- ZVS
 - $V_{IN} < 1/2 V_{OUT}$ – ZVS for all loads
 - $V_{IN} > 1/2 V_{OUT}$ – loss of ZVS
- Low THD is challenging

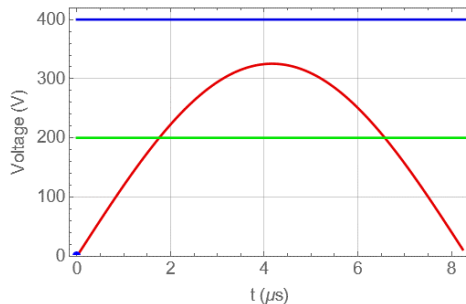
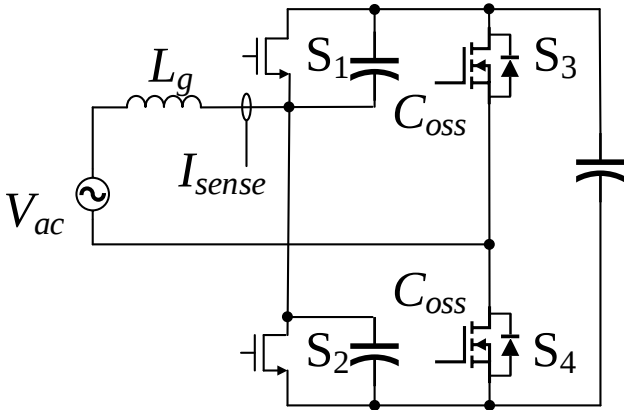
$\left\langle I_{L_g}(t) \right\rangle_{T_s}$ denotes the current in L_g averaged over each switching cycle



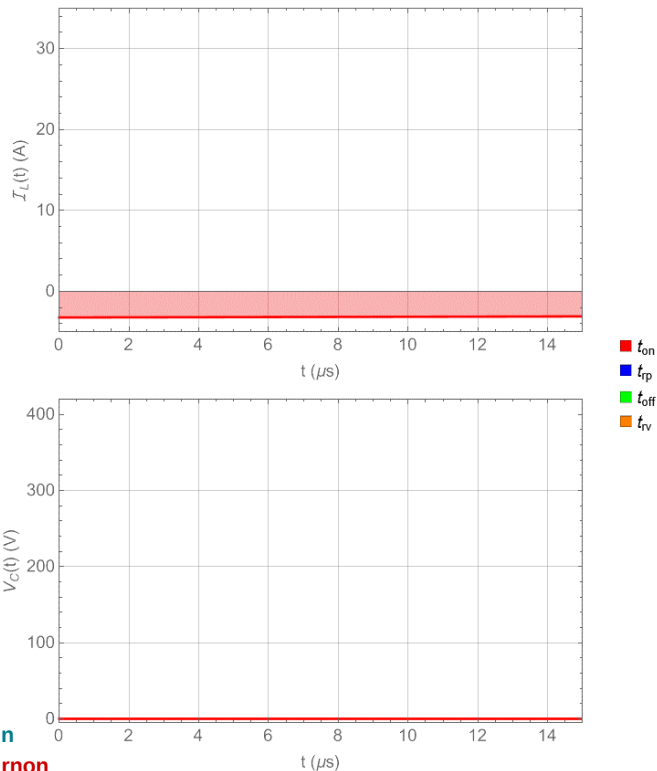
Note: Time base in zoomed plots is relative to: 0.1 ms.

Transition-mode control – ZCD

- Solves the loss of ZVS issue for $V_{IN} > 1/2 V_{OUT}$
- Requires:
 - Precise ZCD
 - Robust algorithm

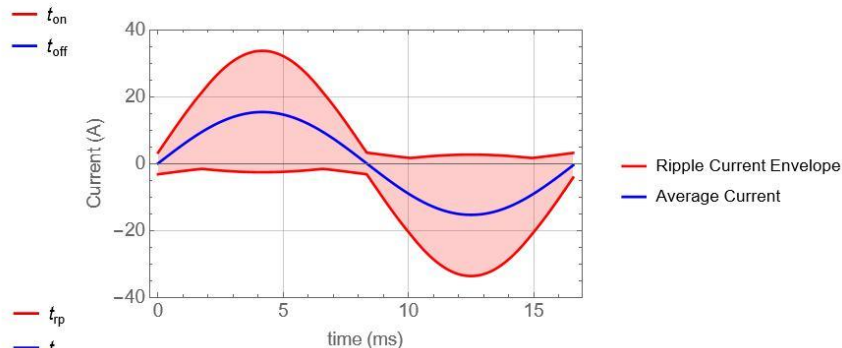
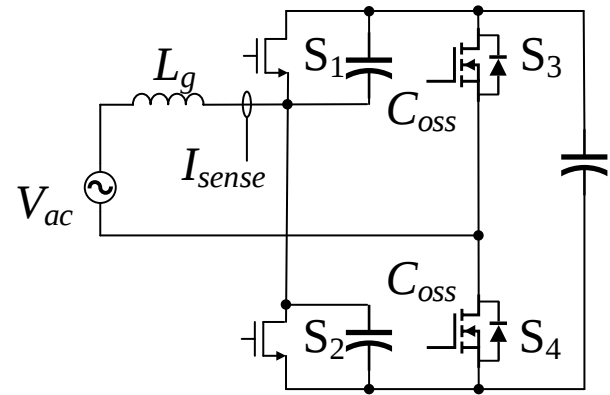
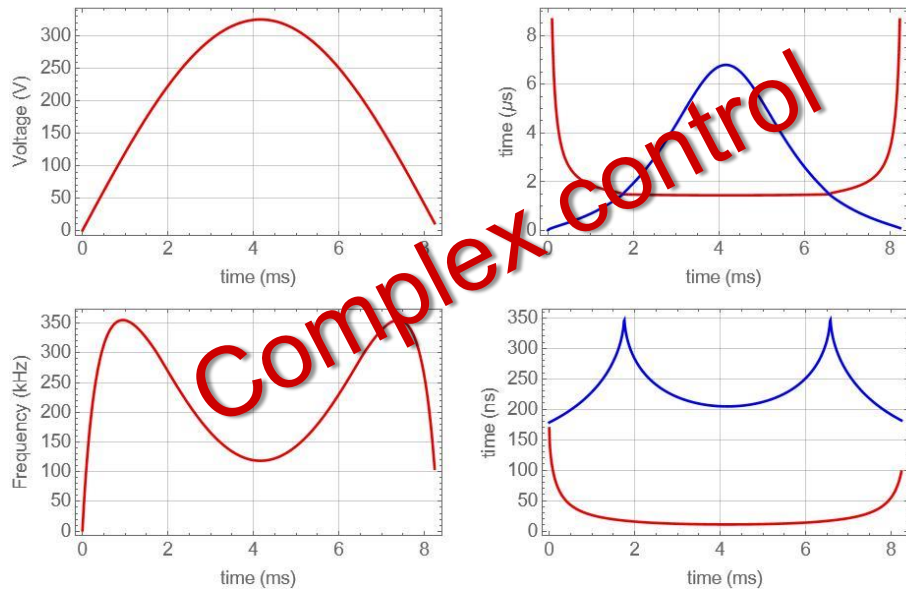


t_{on} – on-time of the control FET
 t_{off} – on-time of the SR
 t_{rp} – dead time between the control FET turnoff and SR turnon
 t_{rv} – dead time between the SR turnoff and the control FET turnon



ZCD solution

- $V_{AC} < 1/2 V_{DC}$ natural ZVS
- $V_{AC} > 1/2 V_{DC}$ additional SR time required
- **Exact timing solution is not available**



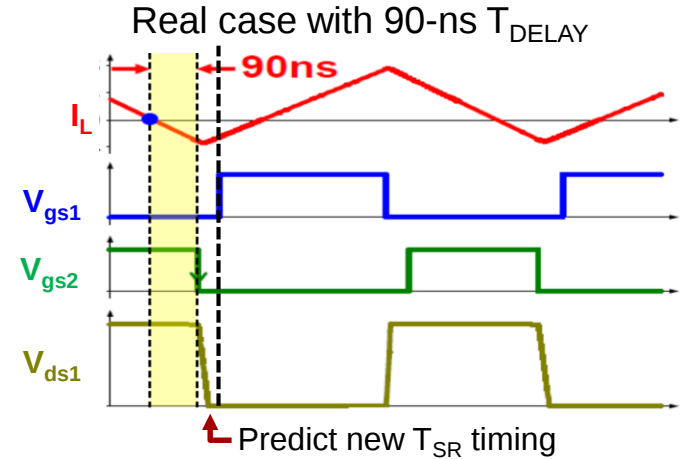
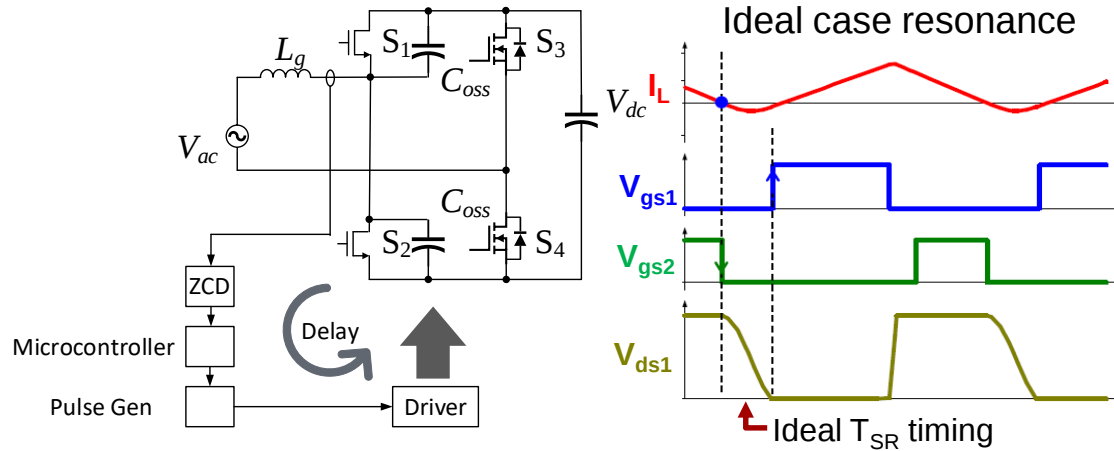
t_{on} – on-time of the control FET

t_{off} – on-time of the SR

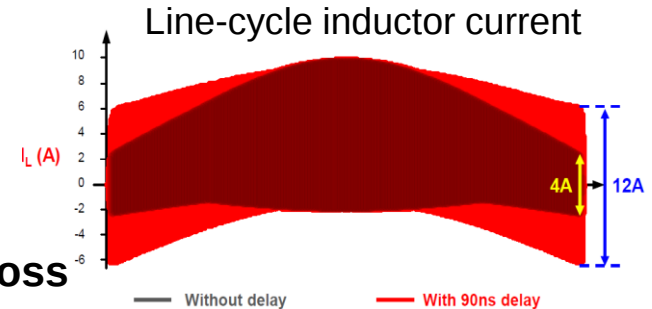
t_{rp} – dead time between the control FET turnoff and SR turnon

t_{rv} – dead time between the SR turnoff and the control FET turnon

ZCD – timing challenge

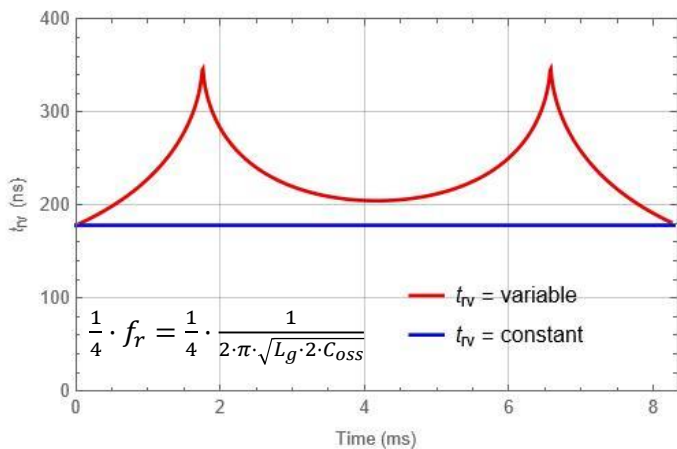


- Need accurate ZCD timing
 - Requires high bandwidth, low delay sensor
 - Delays limit response time
- Requires additional computation to compensate for delays
- **Results in increased THD and unnecessary conduction loss**



Path to solution: Step 1 – simplify timing

- Simplify by making t_{rv} a constant
- Frequency variation is similar
- Ripple current is similar



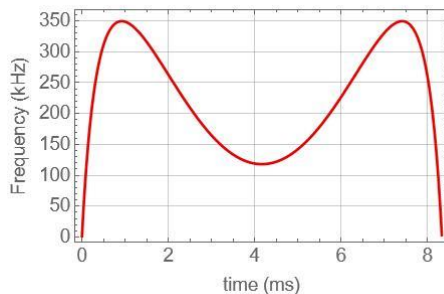
t_{on} – on-time of the control FET

t_{off} – on-time of the SR

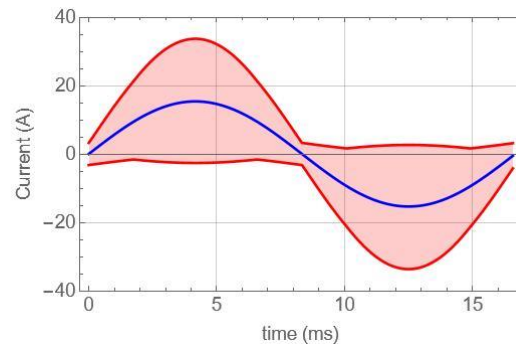
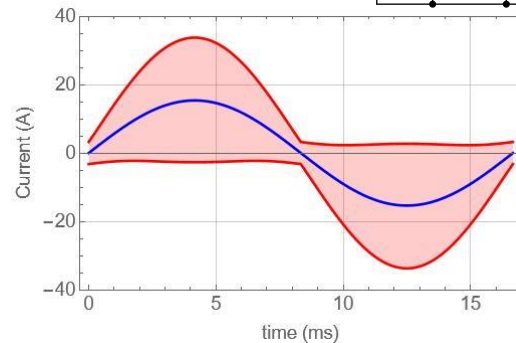
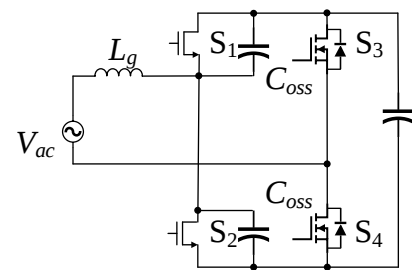
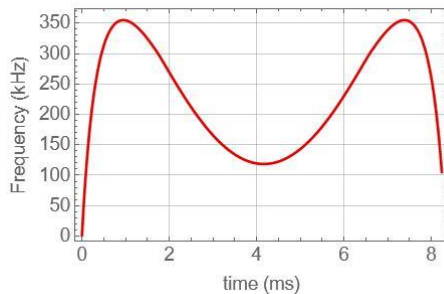
t_{rp} – dead time between the control FET turnoff and SR turnon

t_{rv} – dead time between the SR turnoff and the control FET turnon

Constant t_{rv}

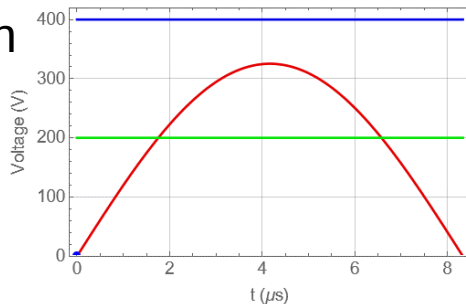
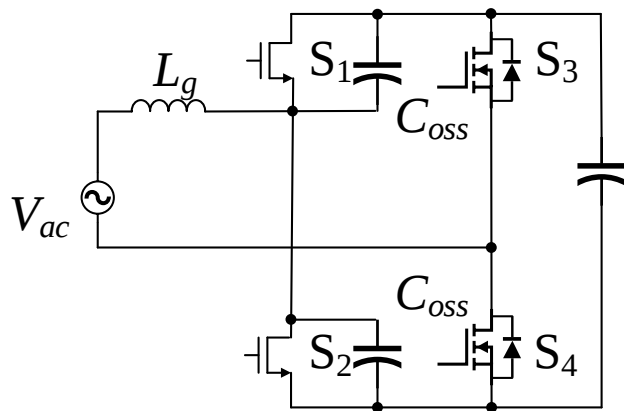


Variable t_{rv}

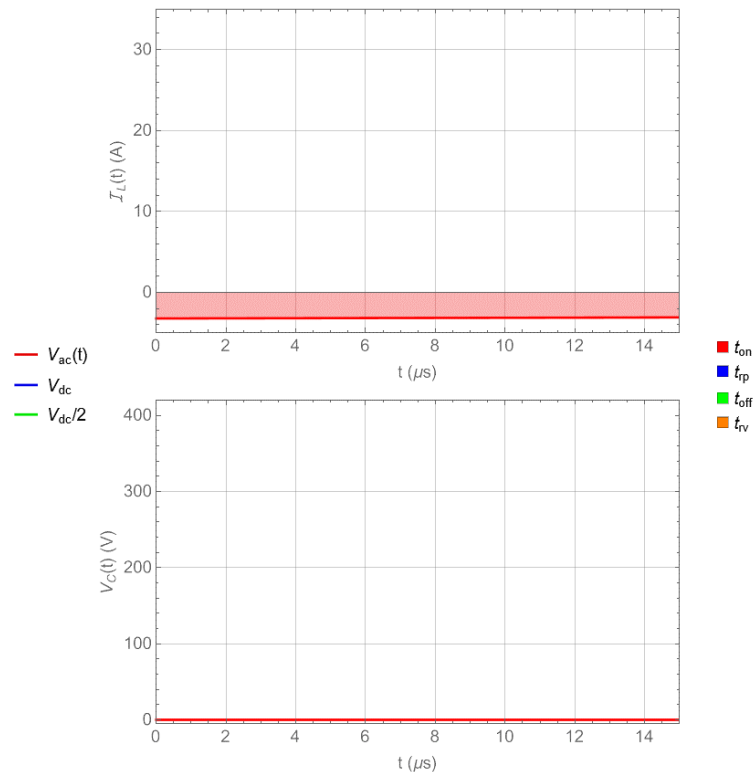


TCM – constant t_{rv}

- No exact solution
- ZVD feedback
 - Eliminates another timing variable
 - Enables an exact solution

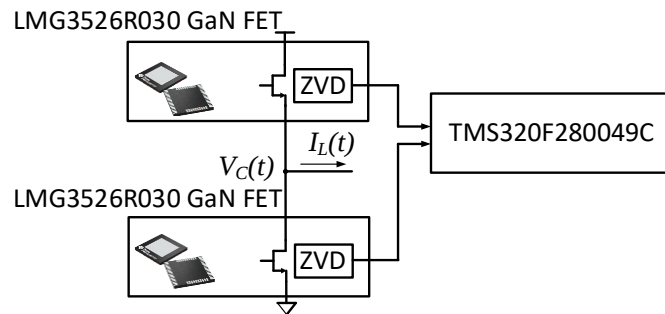


t_{on} – on-time of the **control FET**
 t_{off} – on-time of the **SR**
 t_{rp} – dead time between the **control FET turnoff** and **SR turnon**
 t_{rv} – dead time between the **SR turnoff** and the **control FET turnon**



Path to solution: Step 2 – ZVD feedback

- Status bit output indicating if turned on with ZVS
 - At 500 kHz, the gallium-nitride (GaN) switch achieves ZVS
 - At 1.3 MHz, the GaN switch loses ZVS

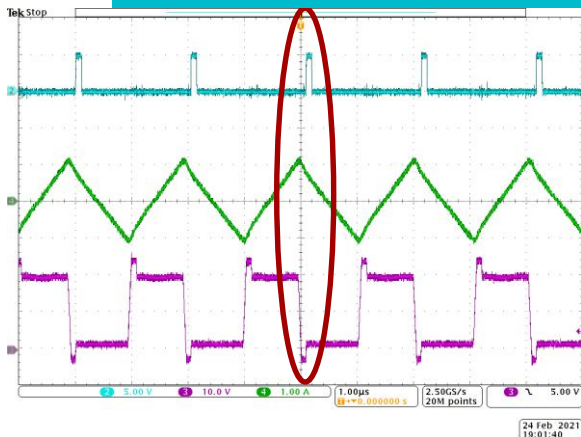


ZVD pulse indicates the achievement of ZVS in the device at turnon

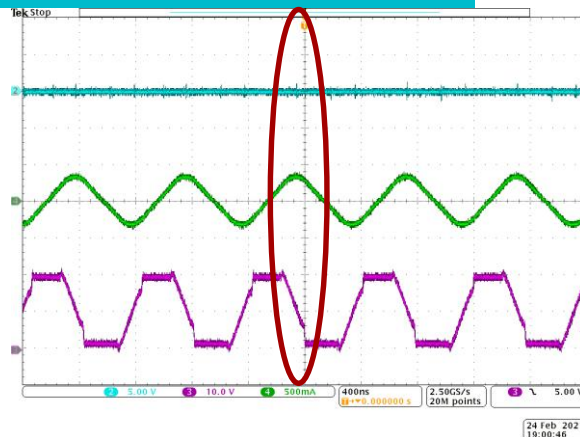
Low-side FET ZVD signal (5 V/div)

I_L (1 A/div)

V_{ds} (10 V/div)

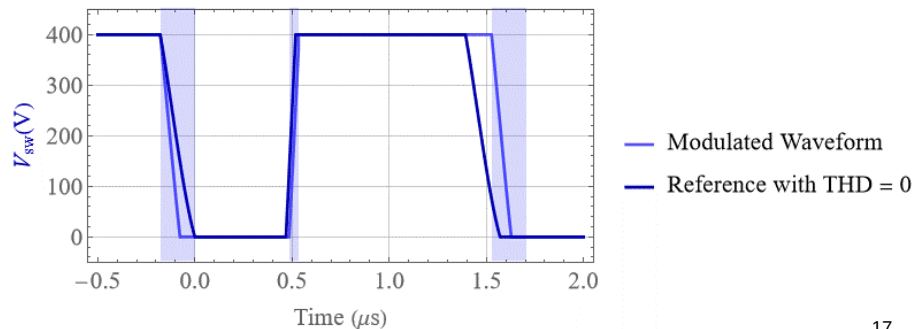
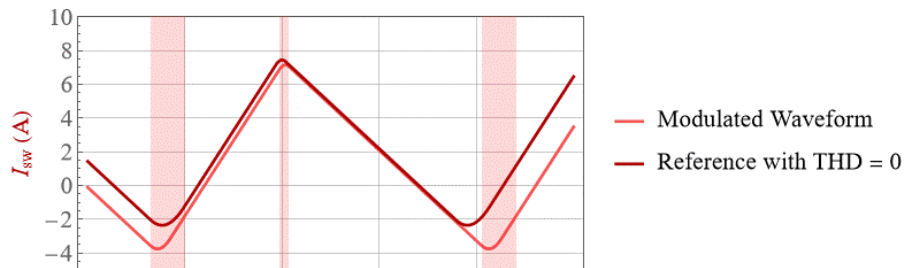
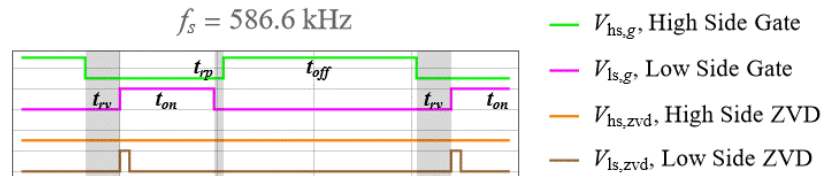
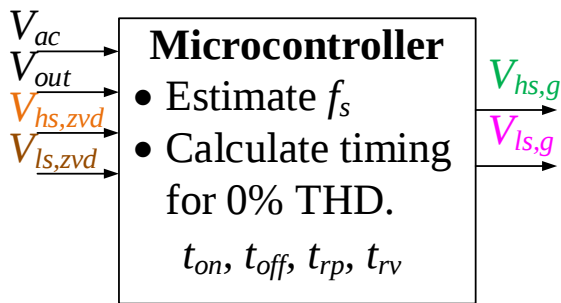
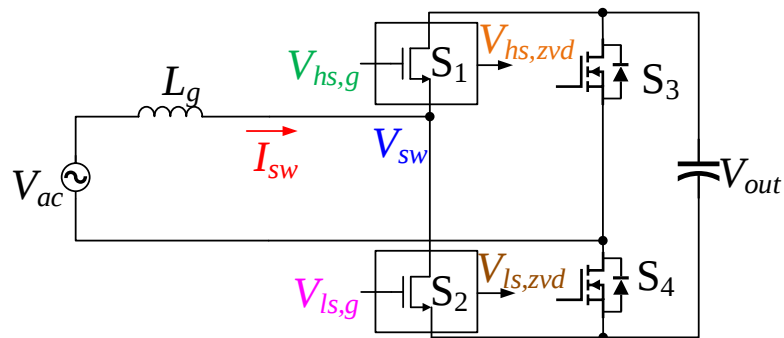


20 V and 500 kHz



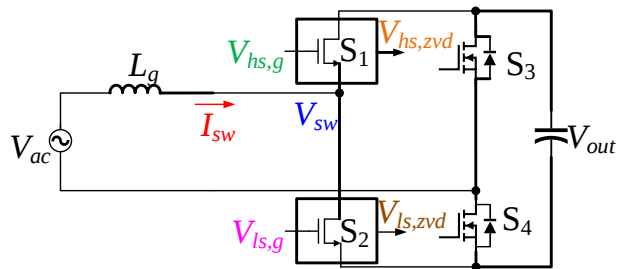
20 V and 1.3 MHz

Exact solution: ZVD feedback and constant t_{rv}



- Reduced control complexity
 - t_{rv} is a constant
 - ZVD feedback determines f_s
- Microcontroller now can force ZVS and unity power factor

Frequency dithering

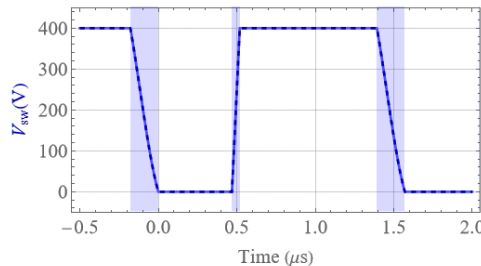
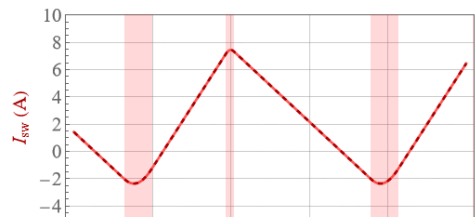
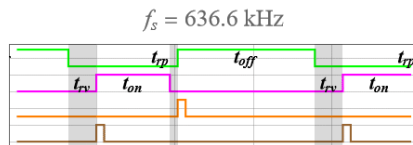


Microcontroller

- Estimate f_s
- Calculate timing for 0% THD.

t_{on} , t_{off} , t_{rp} , t_{rv}

$V_{hs,g}$
 $V_{ls,g}$



— $V_{hs,g}$, High Side Gate

— $V_{ls,g}$, Low Side Gate

— $V_{hs,zvd}$, High Side ZVD

— $V_{ls,zvd}$, Low Side ZVD

— Modulated Waveform

- - - Reference with THD = 0

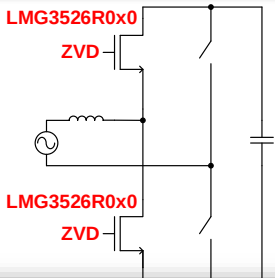
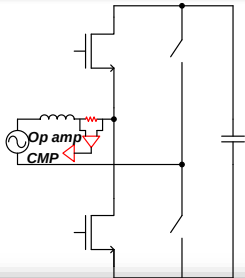
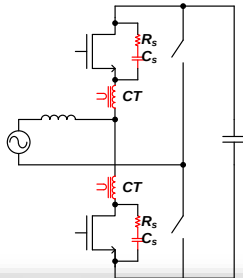
— Modulated Waveform

- - - Reference with THD = 0

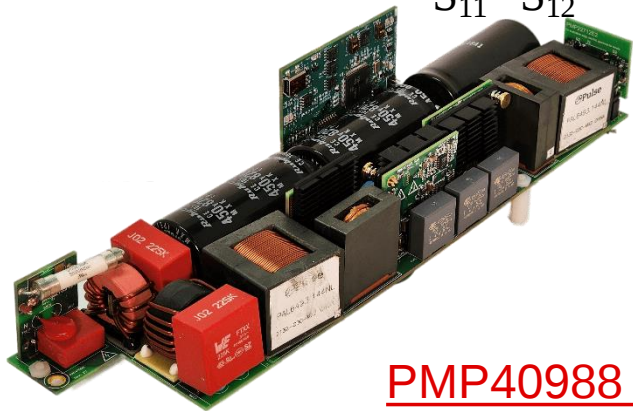
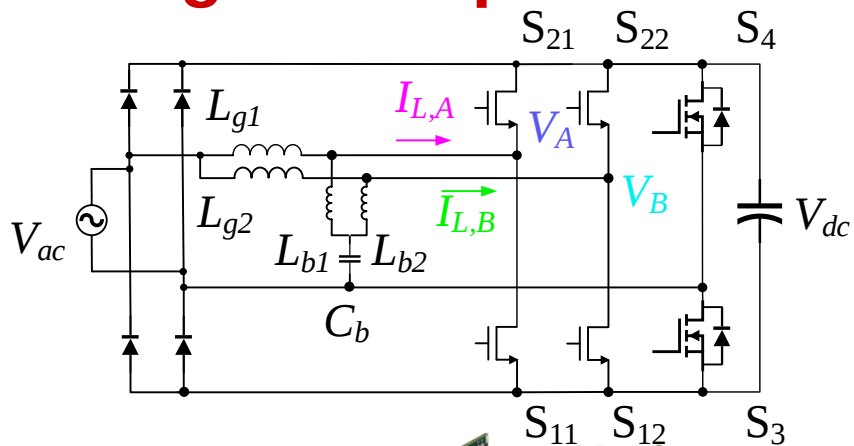
Time (μs)

18

ZVD benefits and comparison to other solutions

	TI GaN ZVD feature LMG3526R0X0	Shunt resistor method	Current transformer method
Circuit diagram			
Periphery circuit	One added channel in isolator	- One shunt resistor, - One high-bandwidth op amp - One fast comparator	- Two current transformers - Two comparators - Clamping circuits: two high-voltage capacitors, two resistors
Periphery circuit cost	\$	\$\$\$	\$
Efficiency impact	No impact	Reduced efficiency caused by shunt loss	Reduced efficiency from current transformer and snubber circuit losses
Footprint size	Almost no added footprint	Large	Large
Control complexity	Simple	Complex	Complex

Design example – 5-kW PFC

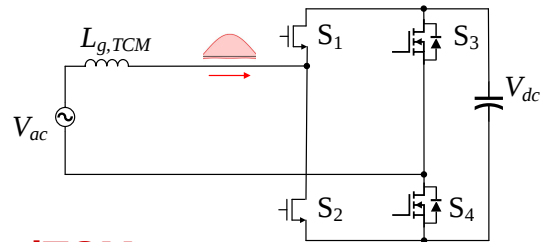


[PMP40988 link](#)

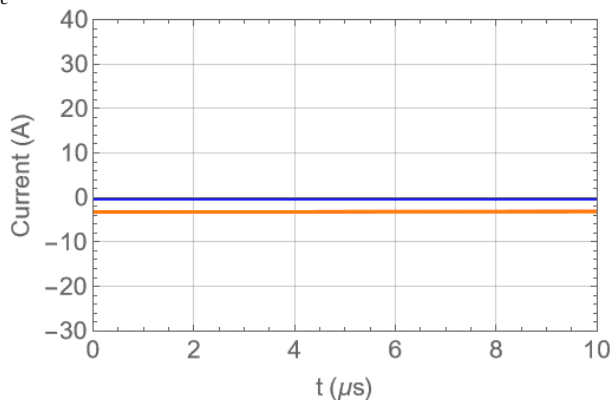
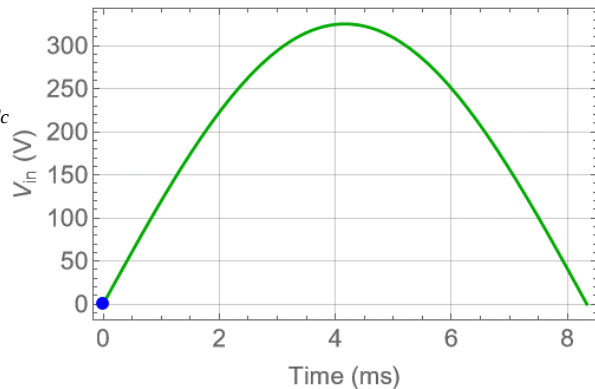
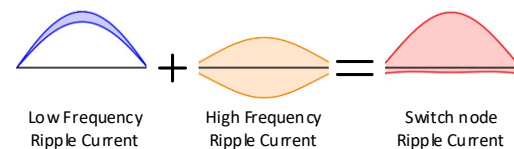
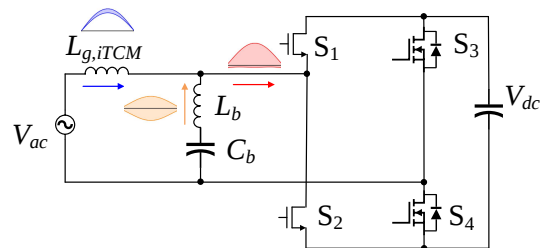
Parameters	Value
AC input	208 V-264 V
Line frequency	50-60 Hz
DC output	400 V
Maximum power	5 kW
Holdup time at full load	20 ms
L_g , low-frequency inductor	140 μ H
L_b , high-frequency inductor	14 μ H
C_b , high-frequency blocking capacitor	1.5 μ F
THD	<5%
EMI	EN55022 Class A
Operating frequency	Variable, 75 kHz-1.2 MHz
Microcontroller	TI: TMS320F280049C
High-frequency GaN FETs (S_{11} , S_{12} , S_{22} , S_{21})	TI: LMG3526R030
Internal dimensions	38 mm $\times$ 65 mm $\times$ 263 mm
Power density	120 W/in ³

iTCM vs. TCM design

TCM



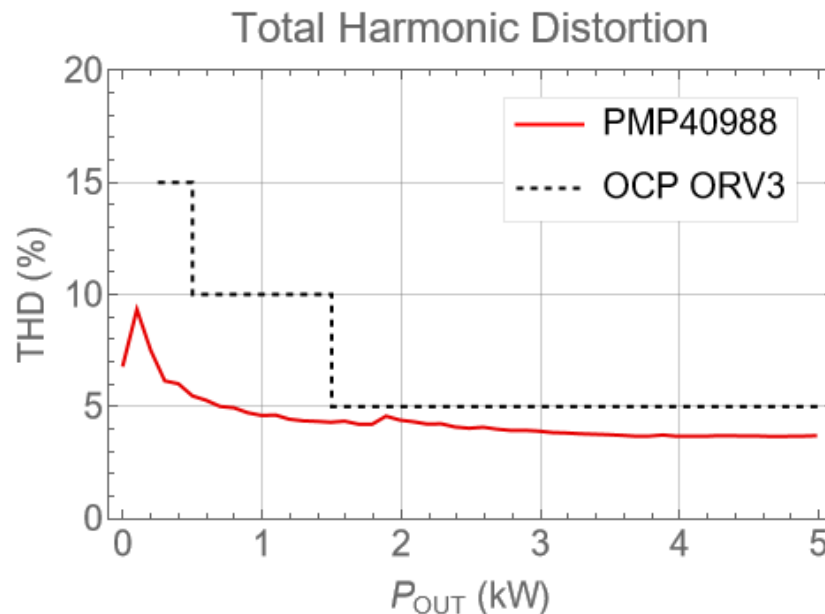
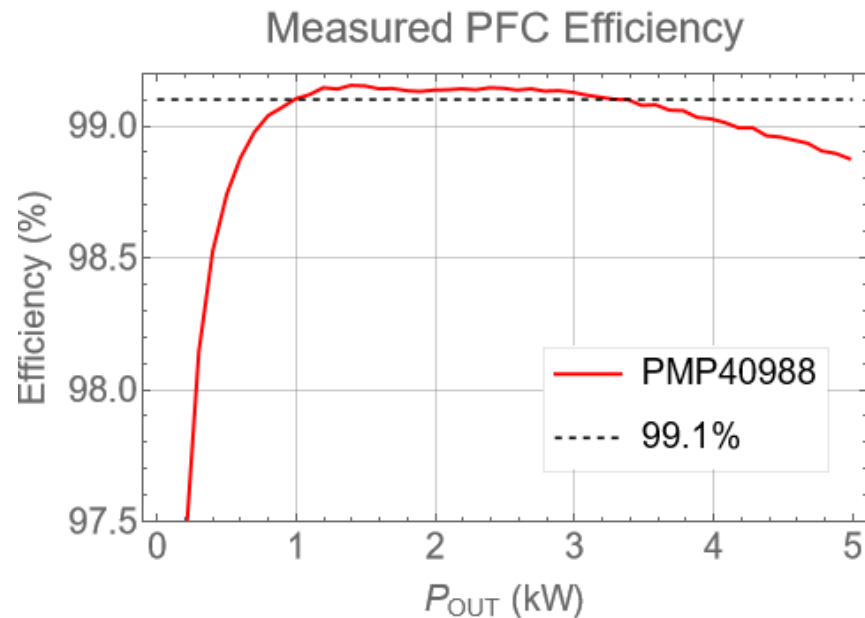
iTCM



iTCM potential benefits

- Optimized inductors
 - L_b (ferrite) – reduced peak currents
 - $L_{g,iTCM}$ inductor (powder iron) – low ripple
 - $L_{g,TCM}$ is ferrite for high-frequency ripple
- Improved differential-mode EMI as high-frequency ripple bypasses input
 - Reduces EMI filter size
 - $L_{g,iTCM}$ forms part of differential-mode filter
- $L_{g,TCM} = L_{g,iTCM} \parallel L_b$

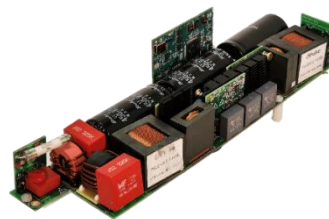
Efficiency and THD with phase shedding



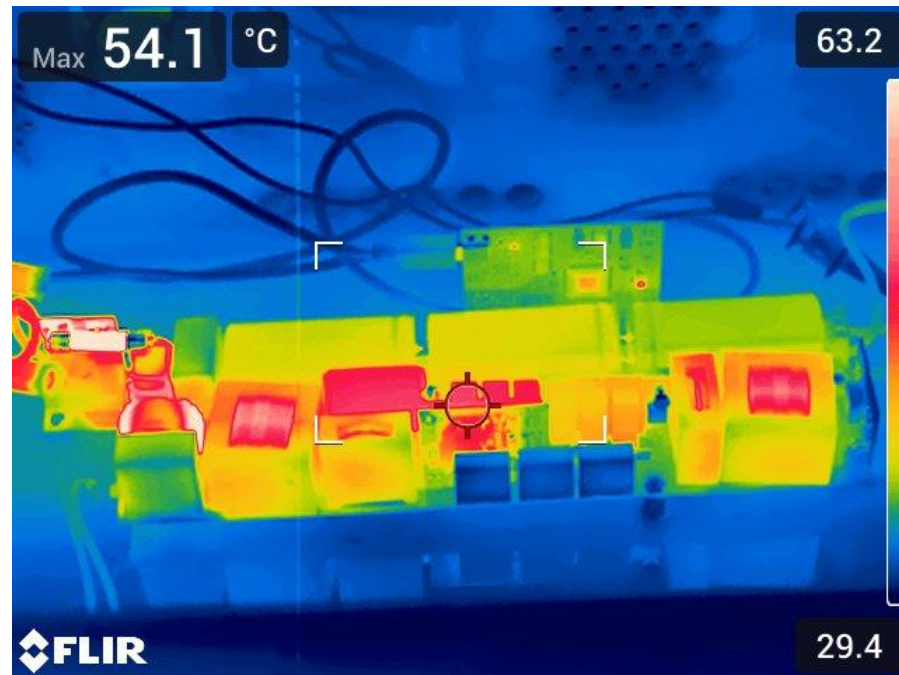
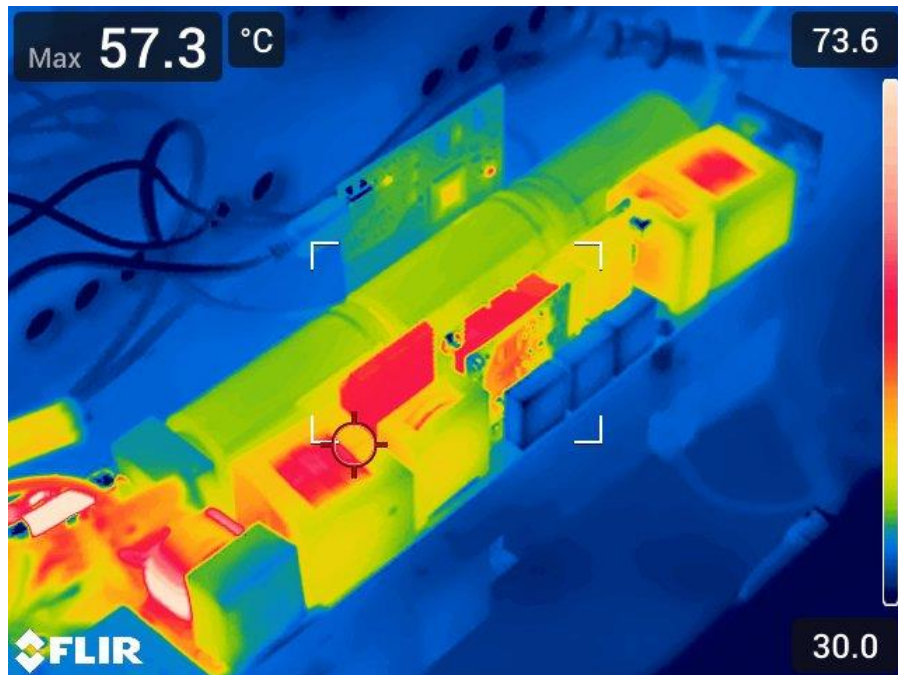
V_{IN} : 230 V

Phase shedding/additional threshold: 1.8 kW

Full-load thermal scan

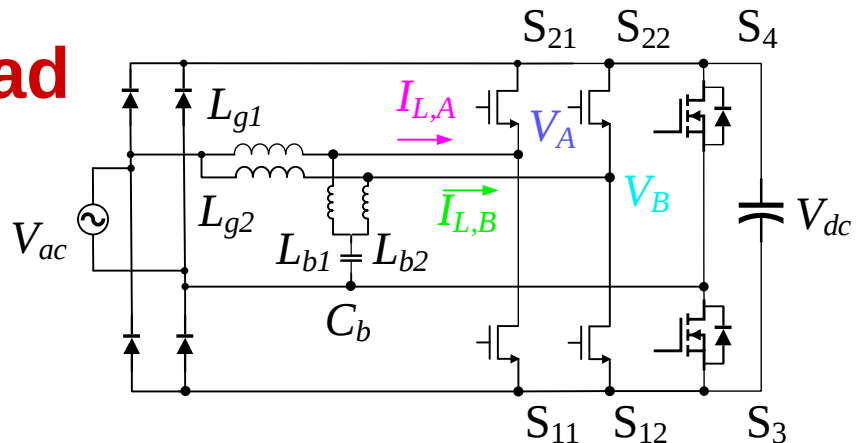


$V_{IN} = 230\text{ V}_{AC}$
 $V_{OUT} = 400\text{ V}$
 $I_{OUT} = 12.5\text{ A}$
38 CFM fan



Experimental results – full load

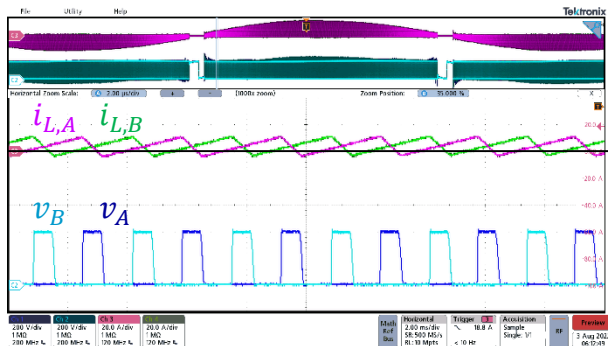
$V_{IN} = 230 \text{ VRMS}$ $V_{OUT} = 400 \text{ V}$ $P = 5 \text{ kW}$



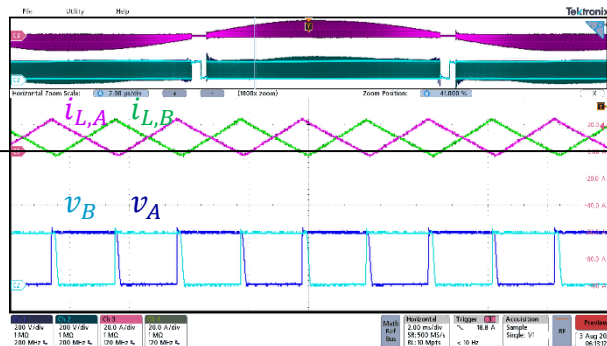
$V_{IN} \ll V_{OUT}/2$

$V_{IN} = V_{OUT}/2$

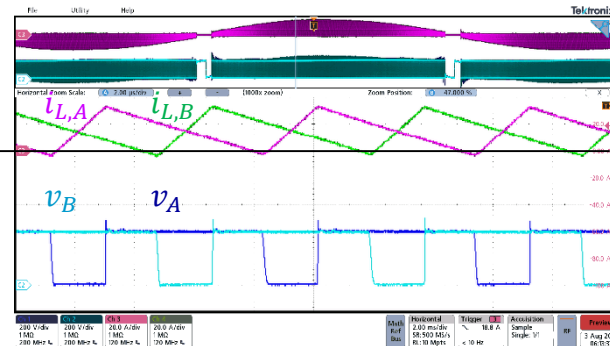
$V_{IN} \gg V_{OUT}/2$



200 V/div, 20 A/div, 2 μ s/div



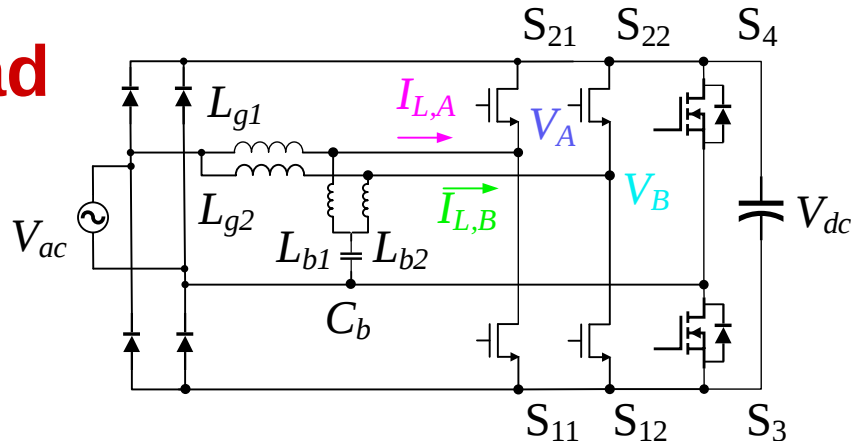
200 V/div, 20 A/div, 2 μ s/div



200 V/div, 20 A/div, 2 μ s/div

Experimental results – no load

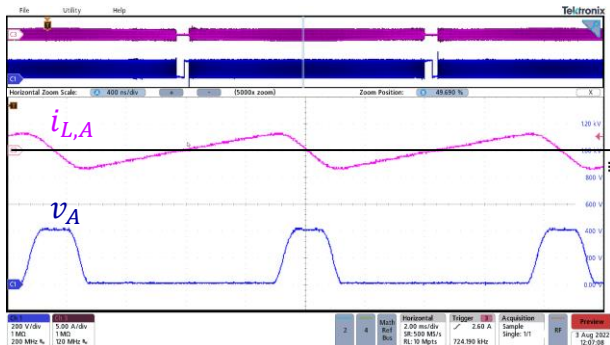
$$V_{IN} = 230 \text{ VRMS} \quad V_{OUT} = 400 \text{ V} \quad P = 0 \text{ kW}$$



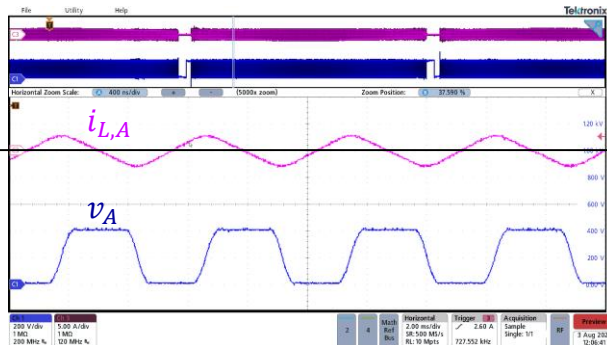
$$V_{IN} \ll V_{OUT}/2$$

$$V_{IN} = V_{OUT}/2$$

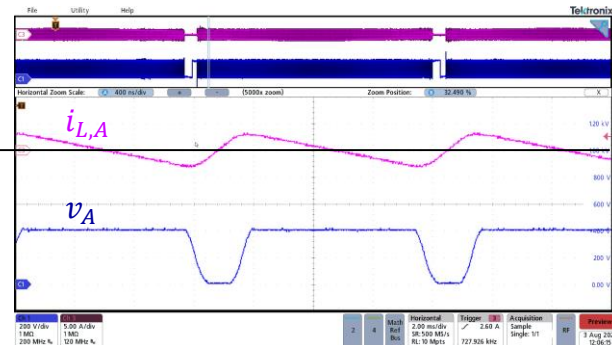
$$V_{IN} \gg V_{OUT}/2$$



200 V/div, 5 A/div, 400 ns/div



200 V/div, 5 A/div, 400 ns/div

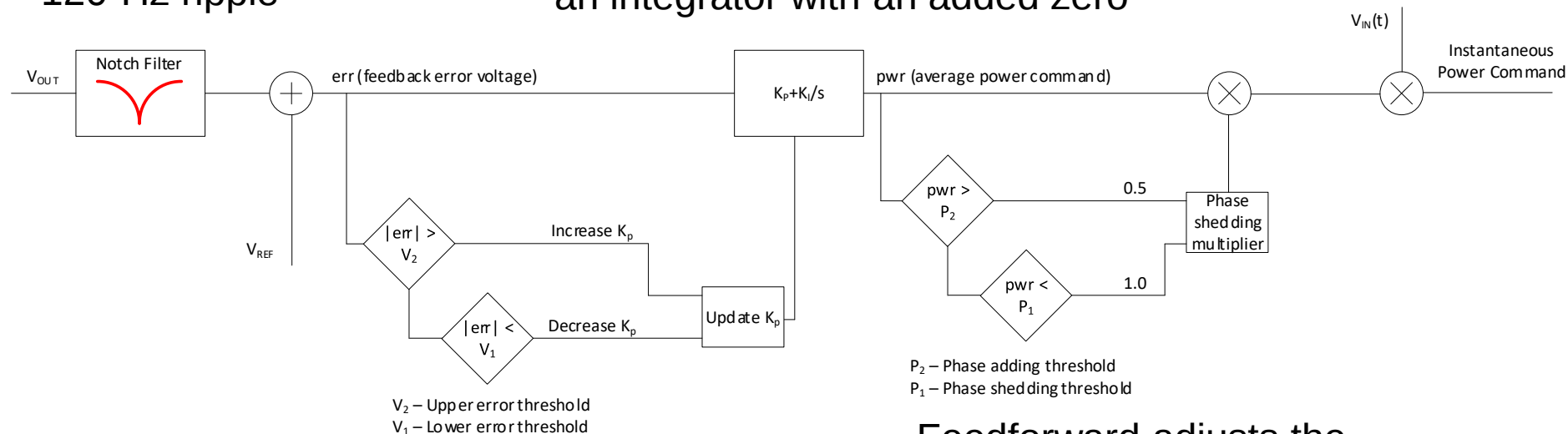


200 V/div, 5 A/div, 400 ns/div

Voltage-loop compensator

Notch filter removes
120-Hz ripple

Standard proportional integral controller equivalent to
an integrator with an added zero



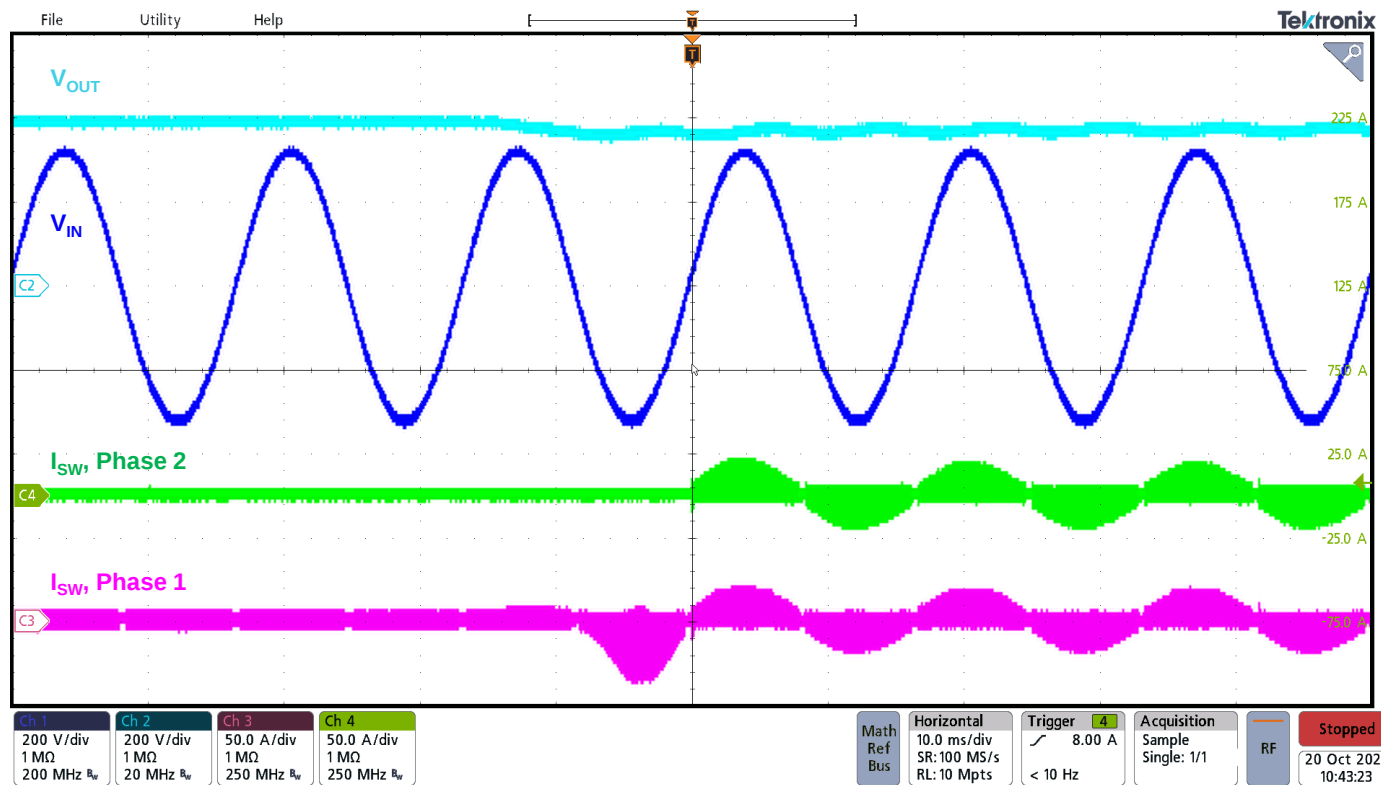
Dynamically change K_p to enable
faster transient response when the
output is far from its target

P_2 – Phase adding threshold
 P_1 – Phase shedding threshold

Feedforward adjusts the
power command to each
phase depending on how
many phases are running

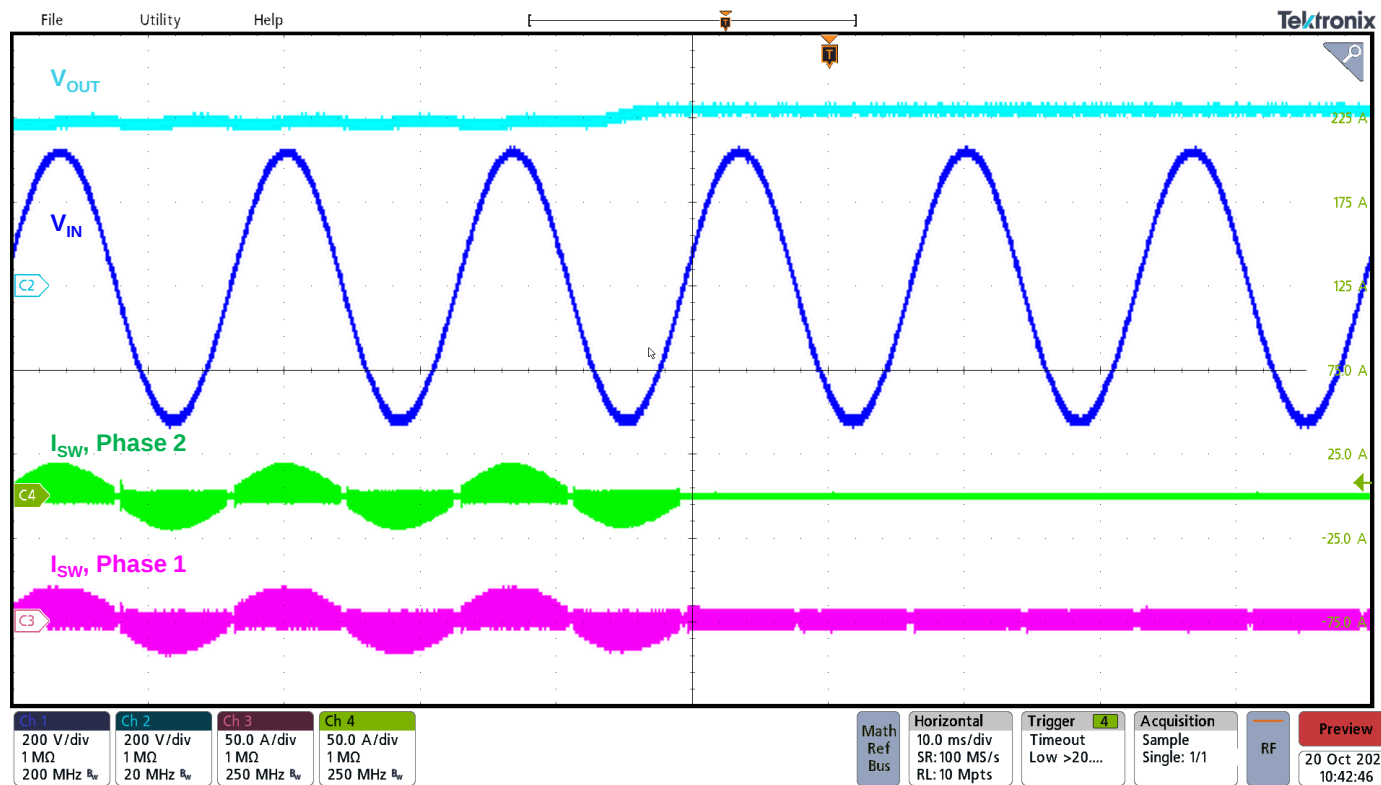
Load transient: 40 W $\rightarrow$ 2.5 kW

$V_{IN} = 230\text{ V}_{AC}$
 $V_{OUT} = 400\text{ V}$
 $I_{OUT} = 0.1\text{ A to } 6.25\text{ A}$



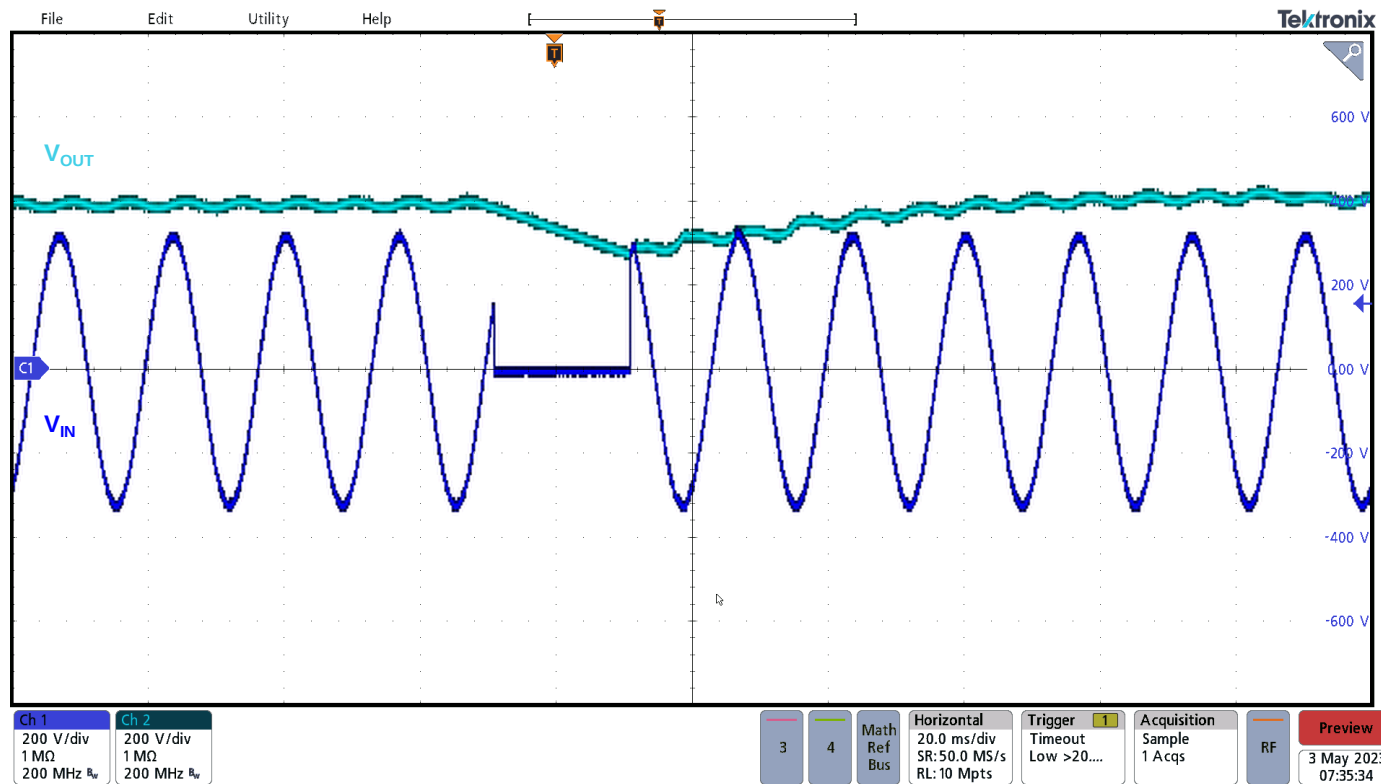
Load transient: 2.5 kW $\rightarrow$ 40 W

$V_{IN} = 230\text{ V}_{AC}$
 $V_{OUT} = 400\text{ V}$
 $I_{OUT} = 6.25\text{ A to }0.1\text{ A}$



AC dropout and restore

$V_{IN} = 230\text{ V}_{AC}$
 $V_{OUT} = 400\text{ V}$
 $I_{OUT} = 12.5\text{ A}$
Dropout = 20 ms
Phase = 30 degrees



Summary and conclusions

- A computationally simple TCM PFC control:
 - Achieves ZVS across the full line and load range
 - Achieves best-in-class THD
 - Requires no control current sensor
- A two-phase interleaved solution using variable frequency and ideal interleaving
 - Efficiency >99.1%
 - THD <5%
- The use of a new ZVD-enabled GaN FET
- ZVD enables the use of a cost-effective C2000™ microcontroller

References

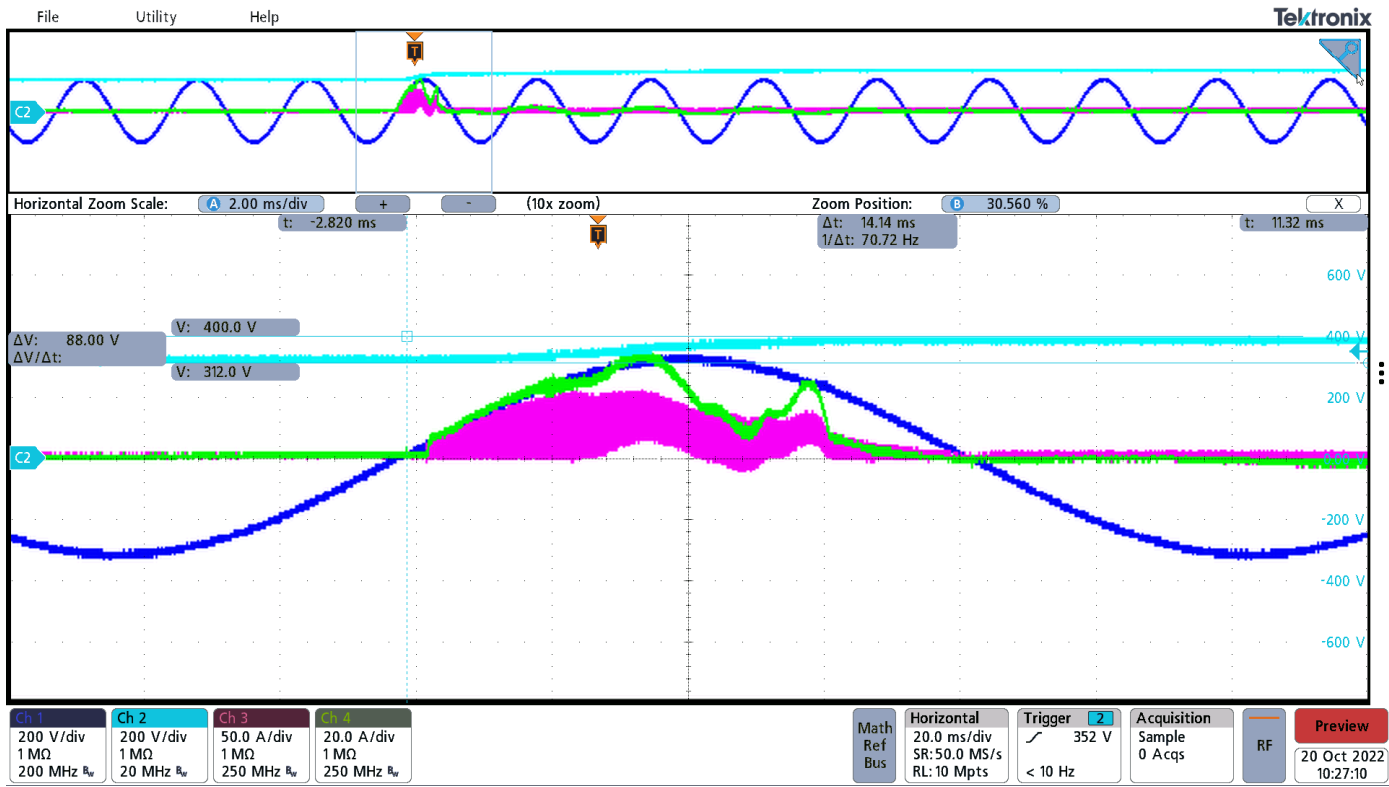
- Fernandes, Ryan, and Olivier Trescases. “A Multimode 1-MHz PFC Front End with Digital Peak Current Modulation.” Published in IEEE Transactions on Power Electronics 31, no. 8 (August 2016): pp. 5694-5708. doi: 10.1109/TPEL.2015.2499194.
- Lim, Shu Fan, and Ashwin M. Khambadkone. “A Multimode Digital Control Scheme for Boost PFC with Higher Efficiency and Power Factor at Light Load.” Published in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Feb. 5-9, 2012, pp. 291-298. doi: 10.1109/APEC.2012.6165833.
- Rothmund, Daniel, Dominik Bortis, Jonas Huber, Davide Biadene, and Johann W. Kolar. “10kV SiC-Based Bidirectional Soft-Switching Single-Phase AC/DC Converter Concept for Medium-Voltage Solid-State Transformers.” Published in 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), April 17-20, 2017, pp. 1-8. doi: 10.1109/PEDG.2017.7972488.
- Liu, Zhengyang. 2017. “Characterization and Application of Wide-Band-Gap Devices for High Frequency Power Conversion.” Ph.D. dissertation, Virginia Polytechnic Institute and State University. <http://hdl.handle.net/10919/77959>.

Backup

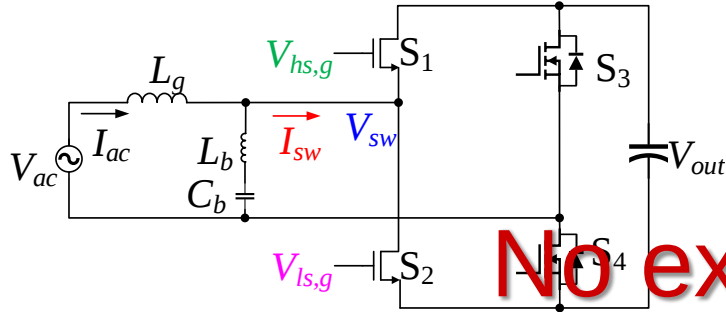
Startup

$$V_{IN} = 230\text{ V}_{AC}$$
$$V_{OUT} = 400\text{ V}$$
$$I_{OUT} = 0\text{ A}$$

CH1 - V_{IN}
CH2 - V_{OUT}
CH3 - I_{SW} master
CH4 - I_{IN}

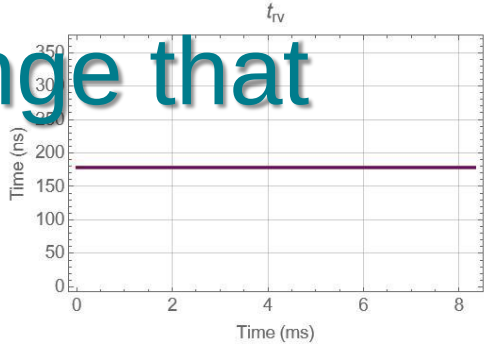
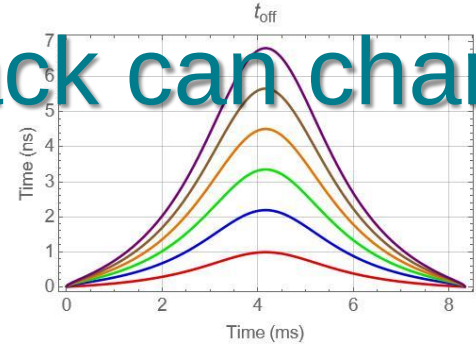
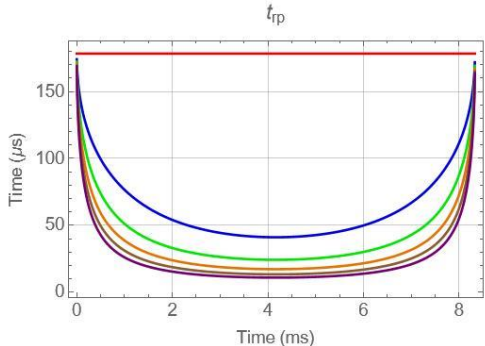
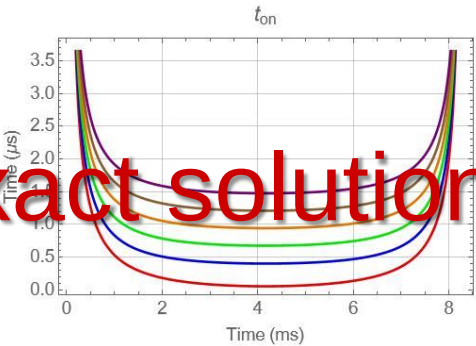
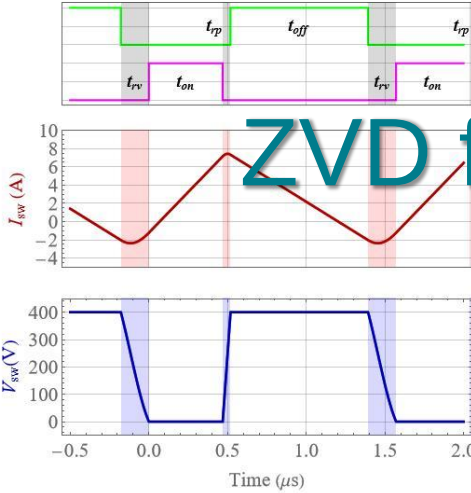


Complete timing solution

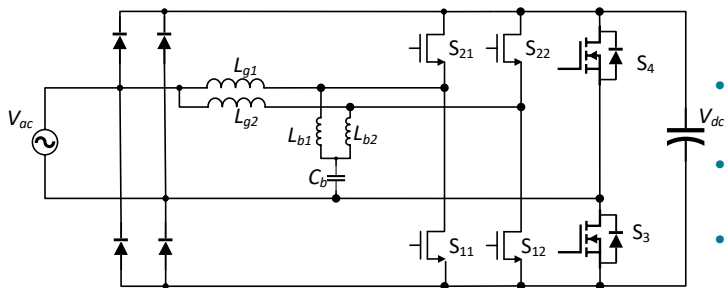


No exact solution

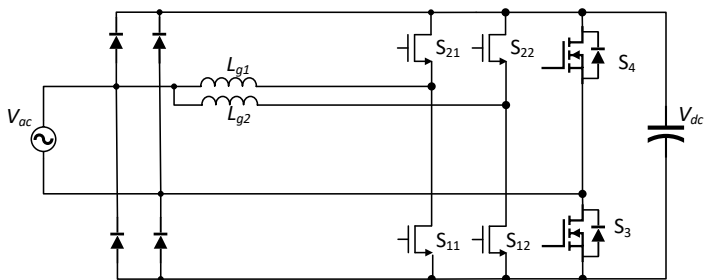
- t_{on} – on-time of the control FET
- t_{off} – on-time of the SR
- t_{rp} – dead time between the control FET turnoff and SR turnon
- t_{rv} – dead time between the SR turnoff and the control FET turnon



iTCM and TCM design equations



- $$L_{g,iTCM} = \frac{V_{g,peak}^2 \cdot (V_{out} - V_{g,peak})}{2 \cdot P \cdot r \cdot V_{out} \cdot f_{min}}$$
- $$L_{b,iTCM} = \frac{V_{g,peak}^2 \cdot (V_{g,peak} - V_{out})}{2 \cdot V_{out} \cdot f_{min} \cdot (P \cdot (r-2) - I_{zvs} \cdot V_{g,peak})}$$
- $$C_{b,iTCM} = \frac{V_{out} \cdot (I_{zvs} \cdot V_{g,peak} - P \cdot (r-2))}{2 \cdot \pi^2 \cdot d \cdot f_{min} \cdot V_{g,peak}^2 \cdot (V_{out} - V_{g,peak})}$$



- $$L_{g,TCM} = \frac{V_{g,peak}^2 \cdot (V_{out} - V_{g,peak})}{2 \cdot V_{out} \cdot f_{min} \cdot (I_{zvs} \cdot V_{g,peak} + 2 \cdot P)}$$

$V_{g,peak}$	$230 \sqrt{2}$	$L_{g,TCM} = \frac{V_{g,peak}^2 (V_{out} - V_{g,peak})}{2 f_{min} V_{out} (I_{zvs} V_{g,peak} + 2 P)}$	11.6604×10^{-6}
V_{out}	400	$L_{g,iTCM} = \frac{V_{g,peak}^2 (V_{out} - V_{g,peak})}{2 P r f_{min} V_{out}}$	131.775×10^{-6}
f_{min}	75 000	$L_{b,iTCM} = \frac{V_{g,peak}^2 (V_{g,peak} - V_{out})}{2 f_{min} V_{out} (P (r-2) - I_{zvs} V_{g,peak})}$	12.7924×10^{-6}
P	5000	$C_{b,iTCM} = \frac{V_{out} (I_{zvs} V_{g,peak} - P (r-2))}{2 \pi^2 d f_{min} V_{g,peak}^2 (V_{out} - V_{g,peak})}$	1.40808×10^{-6}
I_{zvs}	4		
r	0.2		
d	0.25		

- $I_{sw,pk}$ – peak current in the switch
- I_{avg} – cycle-by-cycle average inductor current
- $\Delta I_{L_{g,<i>TCM}}$ – delta I in the inductor
- D – duty cycle
- I_{zvs} – current required for ZVS
- V_{out} – output voltage
- $V_{g,peak}$ – peak AC input voltage
- f_{min} – minimum desired switching frequency
- P – output power
- r – ripple current ratio
- d – impedance ratio



© Copyright 2024 Texas Instruments Incorporated. All rights reserved.

This material is provided strictly “as-is,” for informational purposes only, and without any warranty.
Use of this material is subject to TI’s **Terms of Use**, viewable at [TI.com](https://www.ti.com)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated